

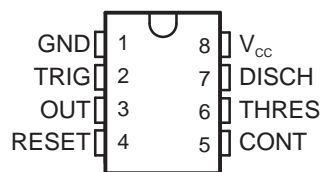
PRECISION TIMERS

 Check for Samples: [NA555](#), [NE555](#), [SA555](#), [SE555](#)

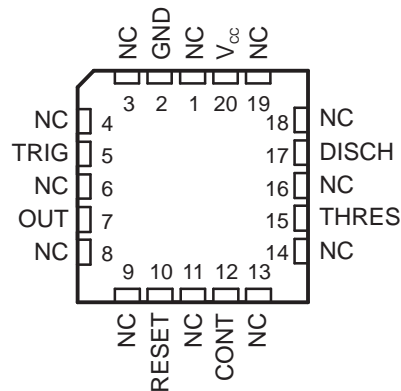
FEATURES

- Timing From Microseconds to Hours
- Astable or Monostable Operation
- Adjustable Duty Cycle
- TTL-Compatible Output Can Sink or Source up to 200 mA

NA555...D OR P PACKAGE
 NE555...D, P, PS, OR PW PACKAGE
 SA555...D OR P PACKAGE
 SE555...D, JG, OR P PACKAGE
 (TOP VIEW)



SE555...FK PACKAGE
 (TOP VIEW)



NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

These devices are precision timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

The threshold and trigger levels normally are two-thirds and one-third, respectively, of V_{CC} . These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set, and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset, and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

The output circuit is capable of sinking or sourcing current up to 200 mA. Operation is specified for supplies of 5 V to 15 V. With a 5-V supply, output levels are compatible with TTL inputs.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION⁽¹⁾

| T _A | V _{THRES MAX} V _{CC} = 15 V | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|--|------------------------|--------------|-----------------------|------------------|
| 0°C to 70°C | 11.2 V | PDIP – P | Tube of 50 | NE555P | NE555P |
| | | SOIC – D | Tube of 75 | NE555D | NE555 |
| | | | Reel of 2500 | NE555DR | |
| | | SOP – PS | Reel of 2000 | NE555PSR | N555 |
| | | TSSOP – PW | Tube of 150 | NE555PW | N555 |
| Reel of 2000 | NE555PWR | | | | |
| –40°C to 85°C | 11.2 V | PDIP – P | Tube of 50 | SA555P | SA555P |
| | | SOIC – D | Tube of 75 | SA555D | SA555 |
| | | | Reel of 2000 | SA555DR | |
| –40°C to 105°C | 11.2 V | PDIP – P | Tube of 50 | NA555P | NA555P |
| | | SOIC – D | Tube of 75 | NA555D | NA555 |
| | | | Reel of 2000 | NA555DR | |
| –55°C to 125°C | 10.6 | PDIP – P | Tube of 50 | SE555P | SE555P |
| | | SOIC – D | Tube of 75 | SE555D | SE555D |
| | | | Reel of 2500 | SE555DR | |
| | | CDIP – JG | Tube of 50 | SE555JG | SE555JG |
| | | LCCC – FK | Tube of 55 | SE555FK | SE555FK |

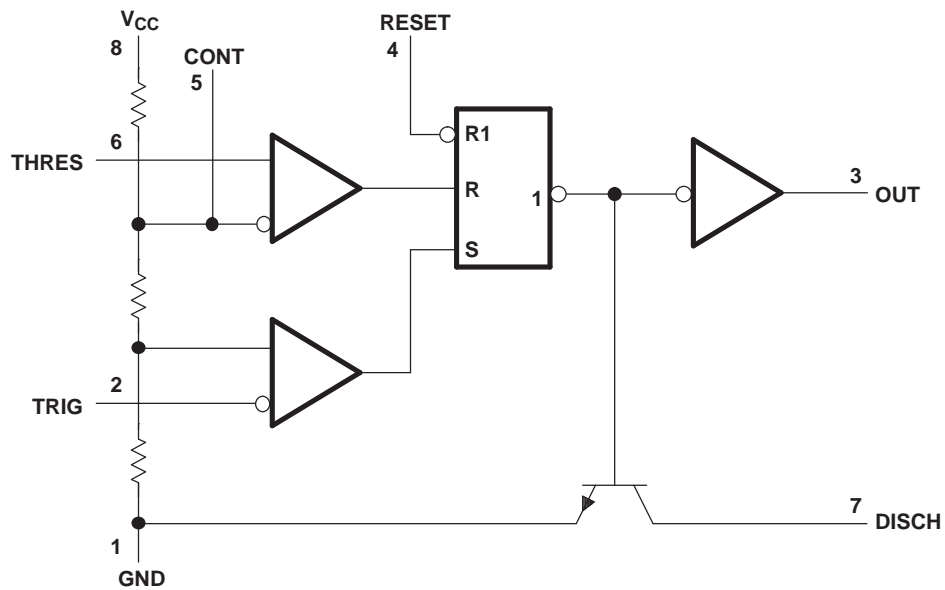
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Table 1. FUNCTION TABLE

| RESET | TRIGGER VOLTAGE ⁽¹⁾ | THRESHOLD VOLTAGE ⁽¹⁾ | OUTPUT | DISCHARGE SWITCH |
|-------|--------------------------------|----------------------------------|---------------------------|------------------|
| Low | Irrelevant | Irrelevant | Low | On |
| High | <1/3 V _{CC} | Irrelevant | High | Off |
| High | >1/3 V _{CC} | >2/3 V _{CC} | Low | On |
| High | >1/3 V _{CC} | <2/3 V _{CC} | As previously established | |

(1) Voltage levels shown are nominal.

FUNCTIONAL BLOCK DIAGRAM



- A. Pin numbers shown are for the D, JG, P, PS, and PW packages.
- B. RESET can override TRIG, which can override THRES.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------|---|--------------------------|------|-----------------|
| V _{CC} | Supply voltage ⁽²⁾ | | 18 | V |
| V _I | Input voltage | CONT, RESET, THRES, TRIG | | V _{CC} |
| I _O | Output current | | ±225 | mA |
| θ _{JA} | Package thermal impedance ^{(3) (4)} | D package | 97 | °C/W |
| | | P package | 85 | |
| | | PS package | 95 | |
| | | PW package | 149 | |
| θ _{JC} | Package thermal impedance ^{(5) (6)} | FK package | 5.61 | °C/W |
| | | JG package | 14.5 | |
| T _J | Operating virtual junction temperature | | 150 | °C |
| | Case temperature for 60 s | FK package | 260 | °C |
| | Lead temperature 1, 6 mm (1/16 in) from case for 60 s | JG package | 300 | °C |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} - T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) Maximum power dissipation is a function of T_{J(max)}, θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case temperature is P_D = (T_{J(max)} - T_C)/θ_{JC}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with MIL-STD-883.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|-----------------|--------------------------------|------------------------------|------|-----------------|
| V _{CC} | Supply voltage | NA555, NE555, SA555 | | V |
| | | 4.5 | 16 | |
| | SE555 | 4.5 | 18 | |
| V _I | Input voltage | CONT, RESET, THRES, and TRIG | | V _{CC} |
| I _O | Output current | | ±200 | mA |
| T _A | Operating free-air temperature | NA555 | -40 | 105 |
| | | NE555 | 0 | 70 |
| | | SA555 | -40 | 85 |
| | | SE555 | -55 | 125 |

Electrical Characteristics

 $V_{CC} = 5\text{ V to }15\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SE555 | | | NA555 NE555 SA555 | | | UNIT |
|--|--|--|-------|------|------|-------------------------|------|------|---------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| THRES voltage level | $V_{CC} = 15\text{ V}$ | | 9.4 | 10 | 10.6 | 8.8 | 10 | 11.2 | V |
| | $V_{CC} = 5\text{ V}$ | | 2.7 | 3.3 | 4 | 2.4 | 3.3 | 4.2 | |
| THRES current ⁽¹⁾ | | | | 30 | 250 | | 30 | 250 | nA |
| TRIG voltage level | $V_{CC} = 15\text{ V}$ | | 4.8 | 5 | 5.2 | 4.5 | 5 | 5.6 | V |
| | | $T_A = -55^\circ\text{C to }125^\circ\text{C}$ | 3 | | 6 | | | | |
| | $V_{CC} = 5\text{ V}$ | | 1.45 | 1.67 | 1.9 | 1.1 | 1.67 | 2.2 | |
| TRIG current | TRIG at 0 V | | | 0.5 | 0.9 | | 0.5 | 2 | μA |
| | $T_A = -55^\circ\text{C to }125^\circ\text{C}$ | | 0.3 | 0.7 | 1 | 0.3 | 0.7 | 1 | V |
| RESET voltage level | RESET at V_{CC} | | | 0.1 | 0.4 | | 0.1 | 0.4 | mA |
| RESET current | RESET at 0 V | | | -0.4 | -1 | | -0.4 | -1.5 | |
| DISCH switch off-state current | | | | 20 | 100 | | 20 | 100 | nA |
| CONT voltage (open circuit) | $V_{CC} = 15\text{ V}$ | | 9.6 | 10 | 10.4 | 9 | 10 | 11 | V |
| | | $T_A = -55^\circ\text{C to }125^\circ\text{C}$ | 9.6 | | 10.4 | | | | |
| | $V_{CC} = 5\text{ V}$ | | 2.9 | 3.3 | 3.8 | 2.6 | 3.3 | 4 | |
| Low-level output voltage | $V_{CC} = 15\text{ V}$, $I_{OL} = 10\text{ mA}$ | | | 0.1 | 0.15 | | 0.1 | 0.25 | V |
| | | $T_A = -55^\circ\text{C to }125^\circ\text{C}$ | | | 0.2 | | | | |
| | $V_{CC} = 15\text{ V}$, $I_{OL} = 50\text{ mA}$ | | | 0.4 | 0.5 | | 0.4 | 0.75 | |
| | | $T_A = -55^\circ\text{C to }125^\circ\text{C}$ | | | 1 | | | | |
| | $V_{CC} = 15\text{ V}$, $I_{OL} = 100\text{ mA}$ | | | 2 | 2.2 | | 2 | 2.5 | |
| | | $T_A = -55^\circ\text{C to }125^\circ\text{C}$ | | | 2.7 | | | | |
| | $V_{CC} = 15\text{ V}$, $I_{OL} = 200\text{ mA}$ | | | 2.5 | | | 2.5 | | |
| | $V_{CC} = 5\text{ V}$, $I_{OL} = 3.5\text{ mA}$ | $T_A = -55^\circ\text{C to }125^\circ\text{C}$ | | | 0.35 | | | | |
| $V_{CC} = 5\text{ V}$, $I_{OL} = 5\text{ mA}$ | | | 0.1 | 0.2 | | 0.1 | 0.35 | | |
| | $T_A = -55^\circ\text{C to }125^\circ\text{C}$ | | | 0.8 | | | | | |
| High-level output voltage | $V_{CC} = 15\text{ V}$, $I_{OL} = -100\text{ mA}$ | | 13 | 13.3 | | 12.75 | 13.3 | V | |
| | | $T_A = -55^\circ\text{C to }125^\circ\text{C}$ | 12 | | | | | | |
| | $V_{CC} = 15\text{ V}$, $I_{OH} = -200\text{ mA}$ | | | 12.5 | | | 12.5 | | |
| | $V_{CC} = 5\text{ V}$, $I_{OL} = -100\text{ mA}$ | | 3 | 3.3 | | 2.75 | 3.3 | | |
| $T_A = -55^\circ\text{C to }125^\circ\text{C}$ | | 2 | | | | | | | |
| Supply current | Output low, No load | $V_{CC} = 15\text{ V}$ | | 10 | 12 | | 10 | 15 | mA |
| | | $V_{CC} = 5\text{ V}$ | | 3 | 5 | | 3 | 6 | |
| | Output high, No load | $V_{CC} = 15\text{ V}$ | | 9 | 10 | | 9 | 13 | |
| | | $V_{CC} = 5\text{ V}$ | | 2 | 4 | | 2 | 5 | |

(1) This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of [Figure 12](#). For example, when $V_{CC} = 5\text{ V}$, the maximum value is $R = R_A + R_B \approx 3.4\text{ M}\Omega$, and for $V_{CC} = 15\text{ V}$, the maximum value is $10\text{ M}\Omega$.

Operating Characteristics

V_{CC} = 5 V to 15 V, T_A = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | SE555 | | | NA555 NE555 SA555 | | | UNIT |
|---|---------------------------------------|--|-------|--------------------|-----|-------------------------|-----|------------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Initial error of timing interval ⁽²⁾ | Each timer, monostable ⁽³⁾ | T _A = 25°C | 0.5 | 1.5 ⁽⁴⁾ | | 1 | 3 | % | |
| | Each timer, astable ⁽⁵⁾ | | 1.5 | | | 2.25 | | | |
| Temperature coefficient of timing interval | Each timer, monostable ⁽³⁾ | T _A = MIN to MAX | 30 | 100 ⁽⁴⁾ | | 50 | | ppm/ °C | |
| | Each timer, astable ⁽⁵⁾ | | 90 | | | 150 | | | |
| Supply-voltage sensitivity of timing interval | Each timer, monostable ⁽³⁾ | T _A = 25°C | 0.05 | 0.2 ⁽⁴⁾ | | 0.1 | 0.5 | %V | |
| | Each timer, astable ⁽⁵⁾ | | 0.15 | | | 0.3 | | | |
| Output-pulse rise time | | C _L = 15 pF, T _A = 25°C | 100 | 200 ⁽⁴⁾ | | 100 | 300 | ns | |
| Output-pulse fall time | | C _L = 15 pF, T _A = 25°C | 100 | 200 ⁽⁴⁾ | | 100 | 300 | ns | |

- (1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
- (2) Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
- (3) Values specified are for a device in a monostable circuit similar to [Figure 9](#), with the following component values: R_A = 2 kΩ to 100 kΩ, C = 0.1 μF.
- (4) On products compliant to MIL-PRF-38535, this parameter is not production tested.
- (5) Values specified are for a device in an astable circuit similar to [Figure 12](#), with the following component values: R_A = 1 kΩ to 100 kΩ, C = 0.1 μF.

TYPICAL CHARACTERISTICS

Data for temperatures below 0°C and above 70°C are applicable for SE555 circuits only.

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

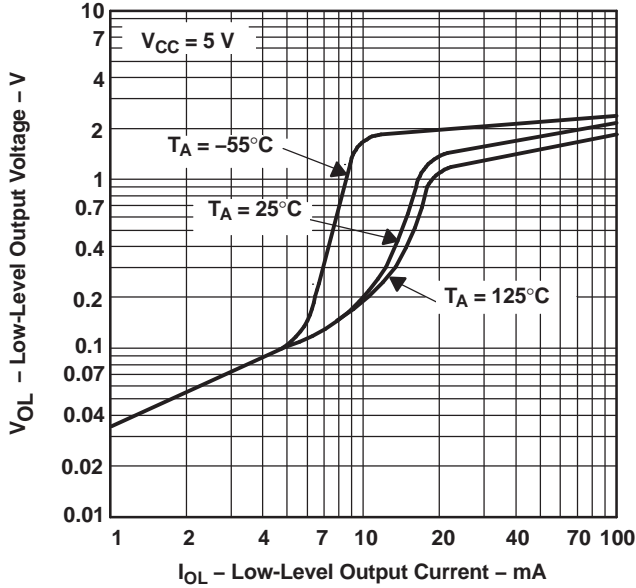


Figure 1.

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

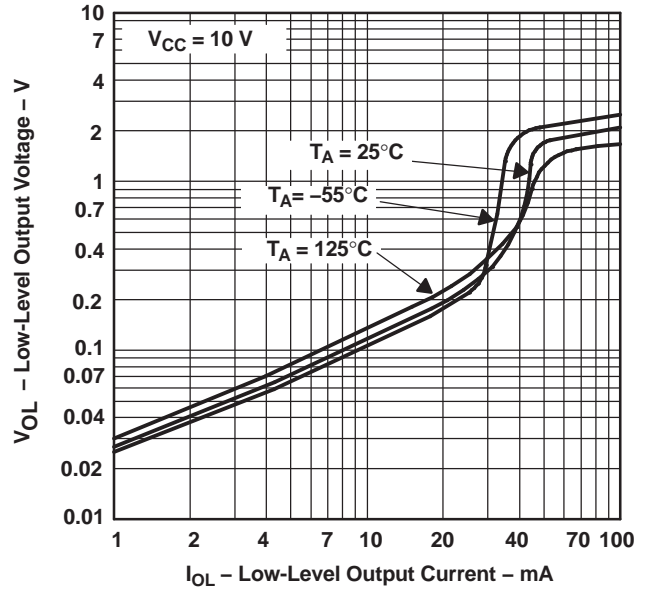


Figure 2.

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

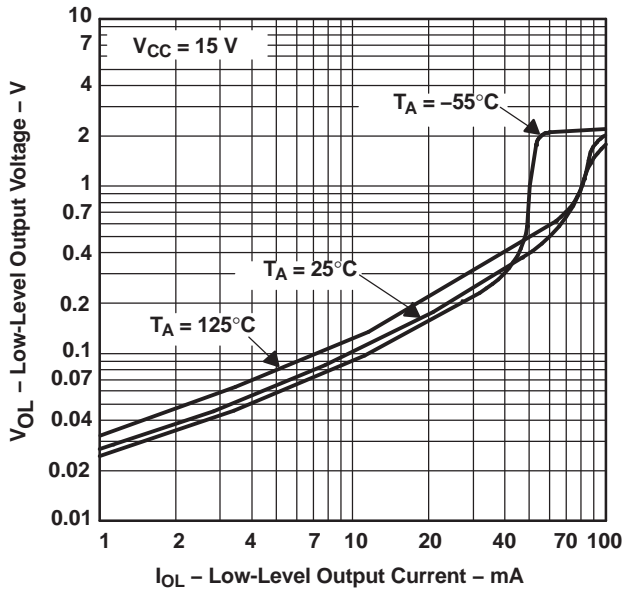


Figure 3.

**DROP BETWEEN SUPPLY VOLTAGE AND OUTPUT
vs
HIGH-LEVEL OUTPUT CURRENT**

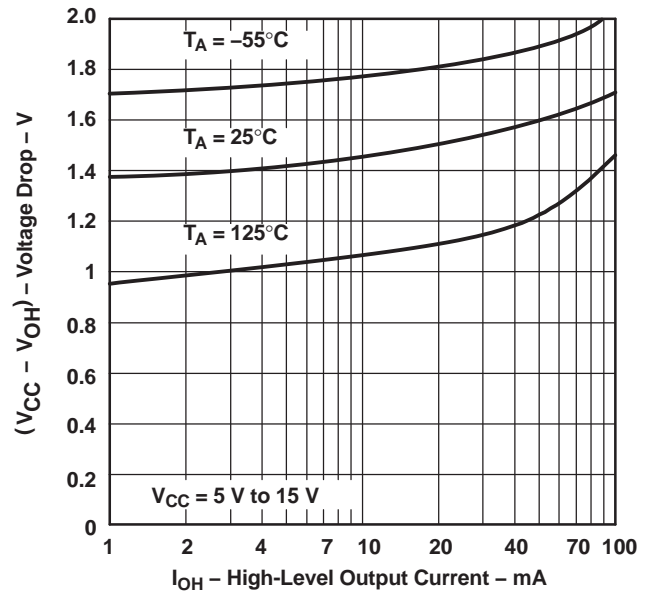


Figure 4.

TYPICAL CHARACTERISTICS (continued)

Data for temperatures below 0°C and above 70°C are applicable for SE555 circuits only.

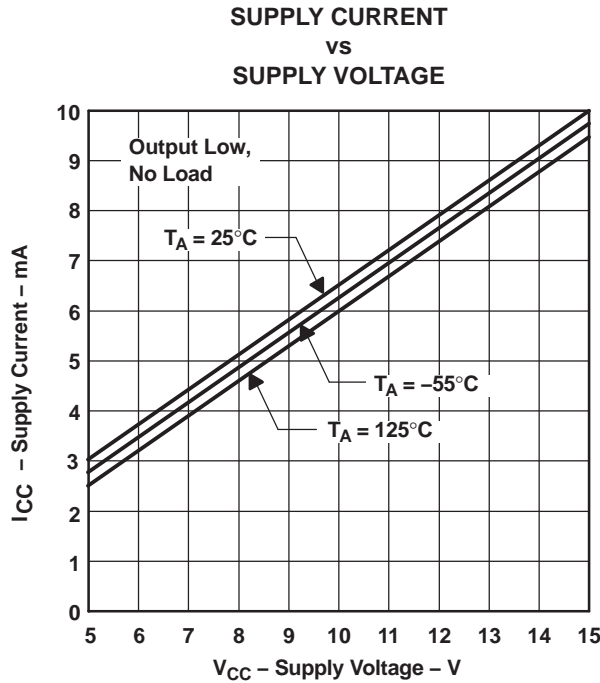


Figure 5.

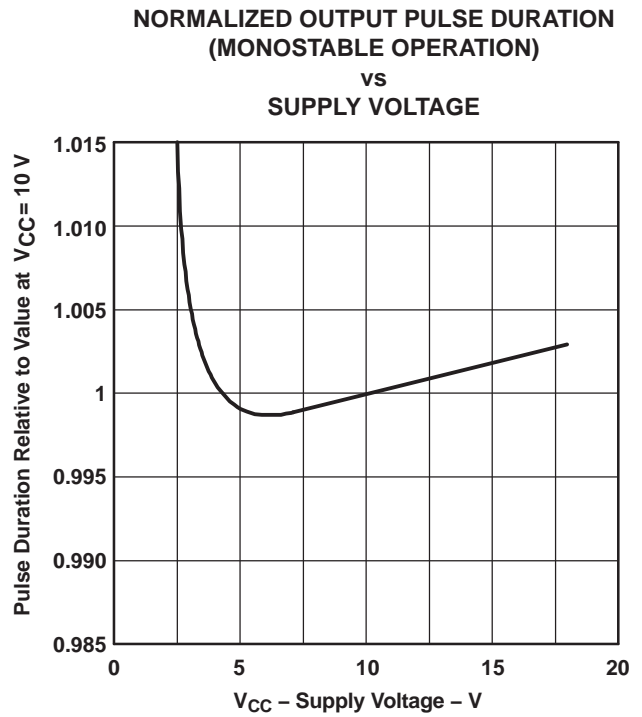


Figure 6.

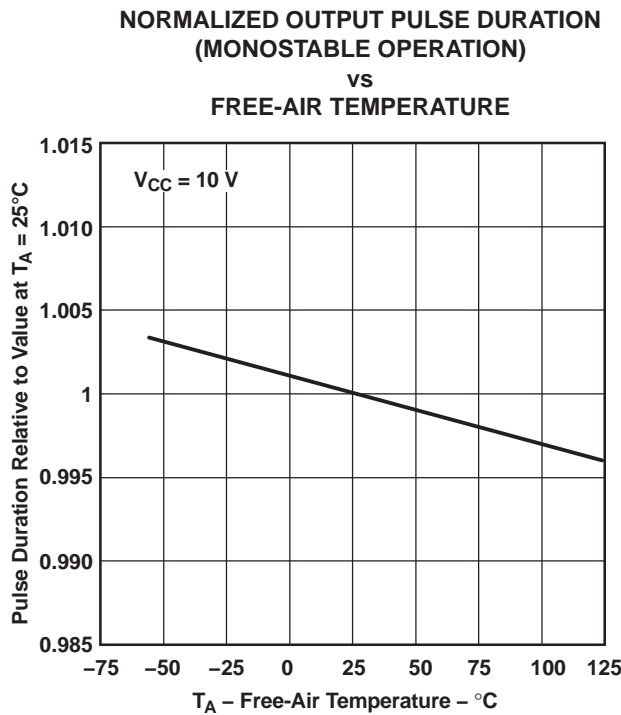


Figure 7.

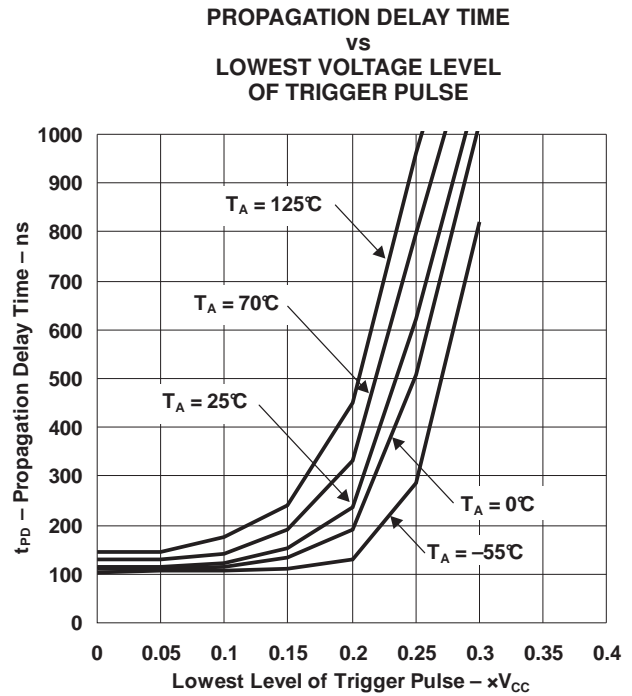
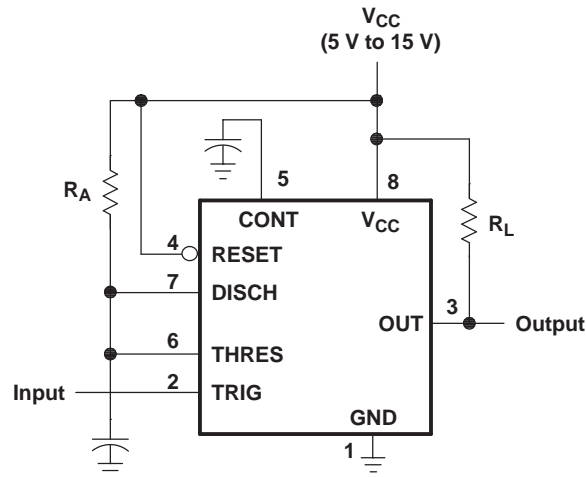


Figure 8.

APPLICATION INFORMATION

Monostable Operation

For monostable operation, any of these timers can be connected as shown in Figure 9. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the flip-flop (\bar{Q} goes low), drives the output high, and turns off Q1. Capacitor C then is charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the flip-flop (\bar{Q} goes high), drives the output low, and discharges C through Q1.



Pin numbers shown are for the D, JG, P, PS, and PW packages.

Figure 9. Circuit for Monostable Operation

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high for at least $10\ \mu\text{s}$ before the end of the timing interval. When the trigger is grounded, the comparator storage time can be as long as $10\ \mu\text{s}$, which limits the minimum monostable pulse width to $10\ \mu\text{s}$. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_w = 1.1R_A C$. Figure 11 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates both are directly proportional to the supply voltage, V_{CC} . The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used, it should be connected to V_{CC} .

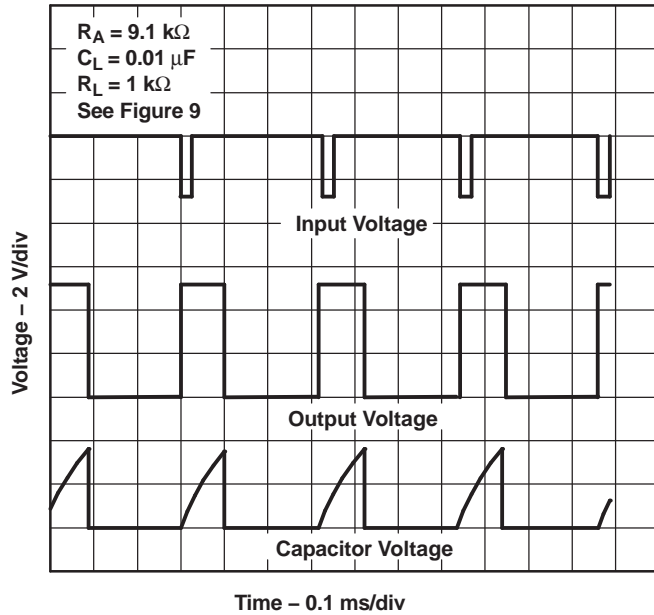


Figure 10. Typical Monostable Waveforms

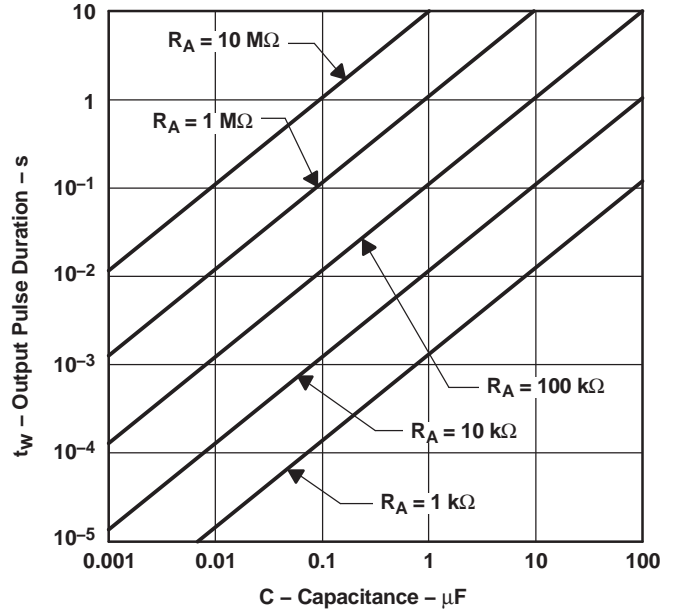
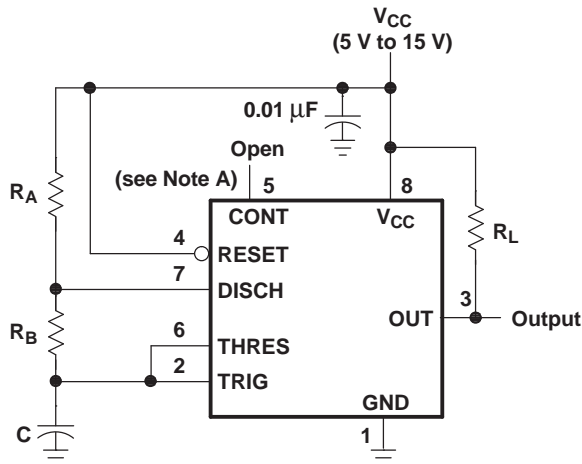


Figure 11. Output Pulse Duration vs Capacitance

Astable Operation

As shown in Figure 12, adding a second resistor, R_B , to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B .

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \times V_{CC}$) and the trigger-voltage level ($\approx 0.33 \times V_{CC}$). As in the monostable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.



Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

Figure 12. Circuit for Astable Operation

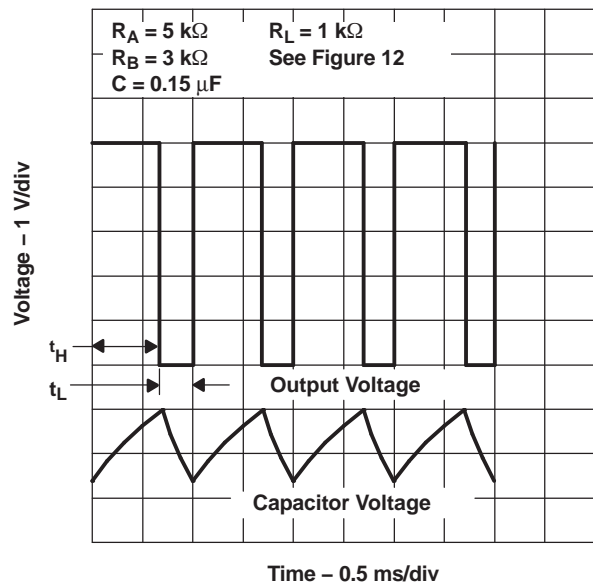


Figure 13. Typical Astable Waveforms

Figure 12 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L can be calculated as follows:

$$t_H = 0.693 (R_A + R_B) C$$

$$t_L = 0.693 (R_B) C$$

Other useful relationships are shown below.

$$\text{period} = t_H + t_L = 0.693 (R_A + 2R_B) C$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B) C}$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B}$$

Output waveform duty cycle

$$= \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B}$$

Figure .

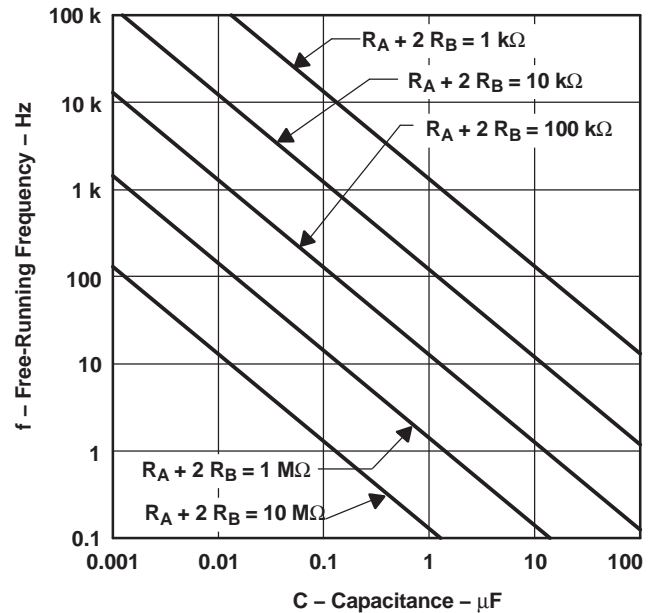
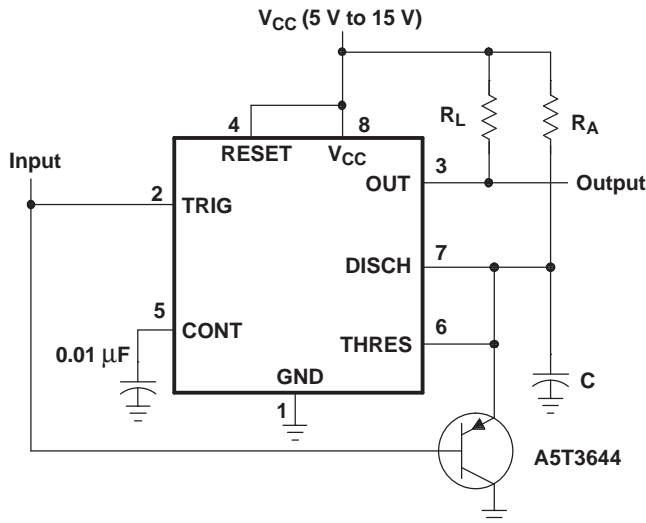


Figure 14. Free-Running Frequency

Missing-Pulse Detector

The circuit shown in Figure 15 can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is retriggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in Figure 16.



Pin numbers shown are shown for the D, JG, P, PS, and PW packages.

Figure 15. Circuit for Missing-Pulse Detector

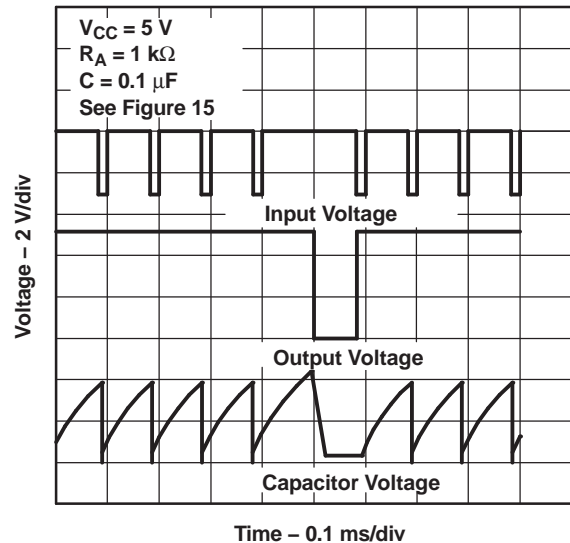


Figure 16. Completed Timing Waveforms for Missing-Pulse Detector

Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of [Figure 9](#) can be made to operate as a frequency divider. [Figure 17](#) shows a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

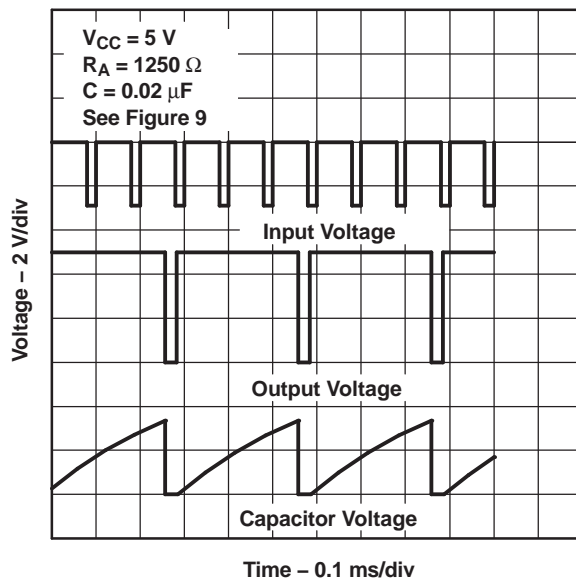
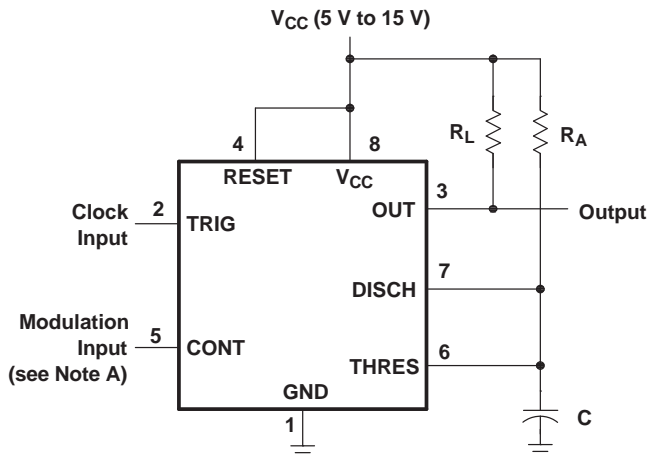


Figure 17. Divide-by-Three Circuit Waveforms

Pulse-Width Modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 18 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 19 shows the resulting output pulse-width modulation. While a sine-wave modulation signal is shown, any wave shape could be used.



Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 18. Circuit for Pulse-Width Modulation

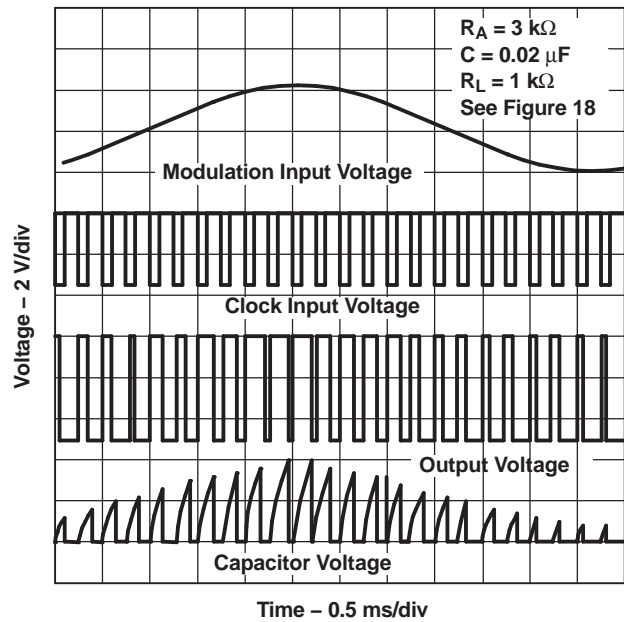
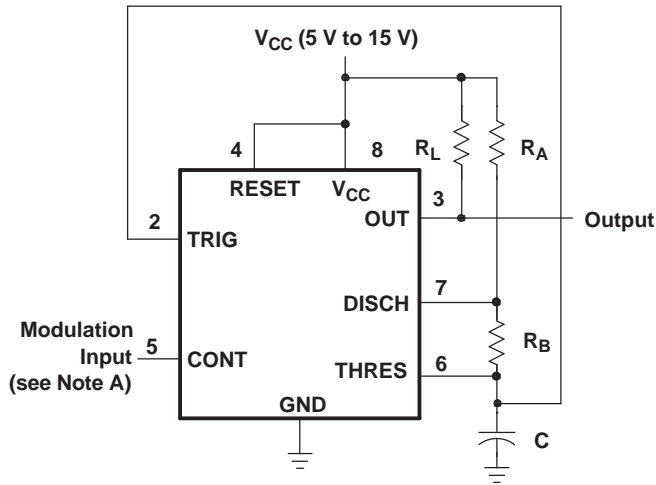


Figure 19. Pulse-Width-Modulation Waveforms

Pulse-Position Modulation

As shown in Figure 20, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and, thereby, the time delay, of a free-running oscillator. Figure 21 shows a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 20. Circuit for Pulse-Position Modulation

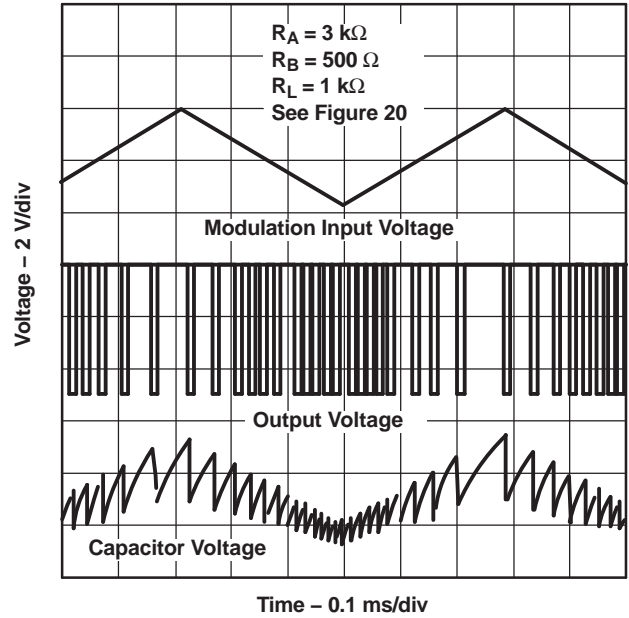
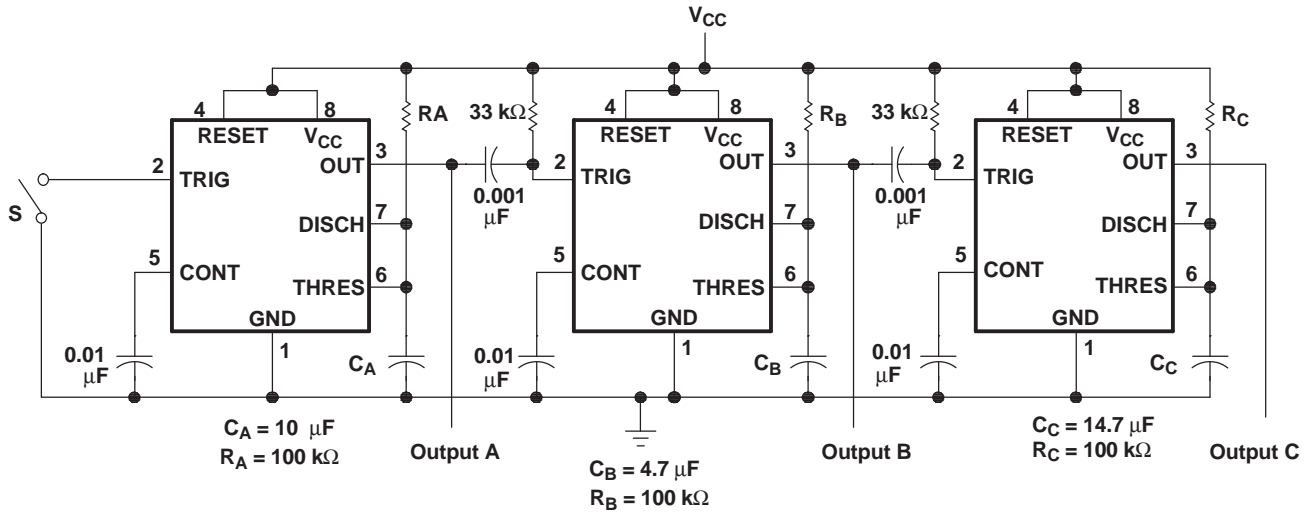


Figure 21. Pulse-Position-Modulation Waveforms

Sequential Timer

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 22 shows a sequencer circuit with possible applications in many systems, and Figure 23 shows the output waveforms.



Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: S closes momentarily at $t = 0$.

Figure 22. Sequential Timer Circuit

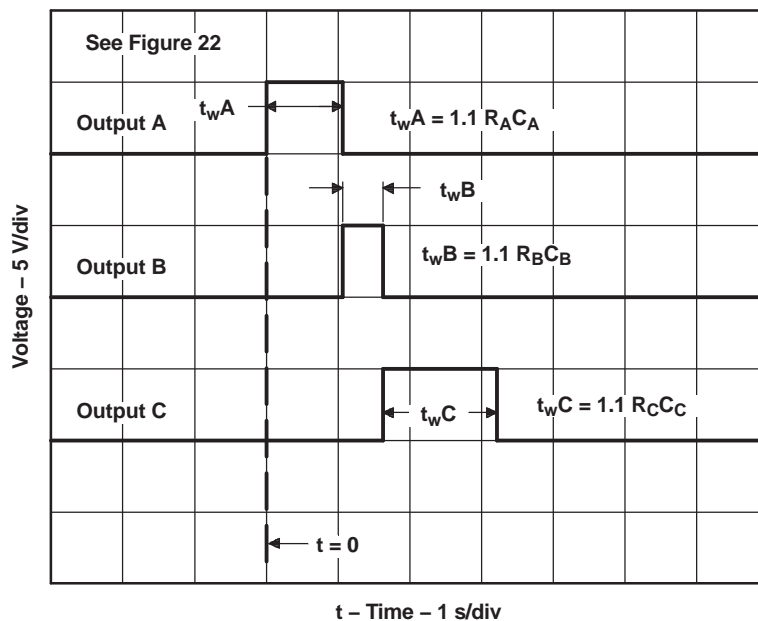


Figure 23. Sequential Timer Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| JM38510/10901BPA | ACTIVE | CDIP | JG | 8 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510 /10901BPA | Samples |
| M38510/10901BPA | ACTIVE | CDIP | JG | 8 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510 /10901BPA | Samples |
| NA555D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | NA555 | Samples |
| NA555DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | NA555 | Samples |
| NA555DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | NA555 | Samples |
| NA555DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | NA555 | Samples |
| NA555P | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 105 | NA555P | Samples |
| NA555PE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 105 | NA555P | Samples |
| NE555D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | NE555 | Samples |
| NE555DE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | NE555 | Samples |
| NE555DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | NE555 | Samples |
| NE555DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | NE555 | Samples |
| NE555DRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | NE555 | Samples |
| NE555DRG3 | PREVIEW | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | 0 to 70 | NE555 | |
| NE555DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | NE555 | Samples |
| NE555P | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | NE555P | Samples |
| NE555PE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | NE555P | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| NE555PSLE | OBSOLETE | SO | PS | 8 | | TBD | Call TI | Call TI | 0 to 70 | | |
| NE555PSR | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | N555 | Samples |
| NE555PSRE4 | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | N555 | Samples |
| NE555PSRG4 | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | N555 | Samples |
| NE555PW | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | N555 | Samples |
| NE555PWE4 | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | N555 | Samples |
| NE555PWG4 | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | N555 | Samples |
| NE555PWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | N555 | Samples |
| NE555PWRE4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | N555 | Samples |
| NE555PWRG4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | N555 | Samples |
| NE555Y | OBSOLETE | | | 0 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SA555D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | SA555 | Samples |
| SA555DE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | SA555 | Samples |
| SA555DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | SA555 | Samples |
| SA555DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | SA555 | Samples |
| SA555DRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | SA555 | Samples |
| SA555DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | SA555 | Samples |
| SA555P | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SA555P | Samples |
| SA555PE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SA555P | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| SE555D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | SE555 | Samples |
| SE555DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | SE555 | Samples |
| SE555DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | SE555 | Samples |
| SE555DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | SE555 | Samples |
| SE555FKB | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SE555FKB | Samples |
| SE555JG | ACTIVE | CDIP | JG | 8 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SE555JG | Samples |
| SE555JGB | ACTIVE | CDIP | JG | 8 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SE555JGB | Samples |
| SE555N | OBSOLETE | PDIP | N | 8 | | TBD | Call TI | Call TI | -55 to 125 | | |
| SE555P | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | SE555P | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF SE555, SE555M :

- Catalog: [SE555](#)
- Military: [SE555M](#)
- Space: [SE555-SP](#), [SE555-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| NA555DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| NA555DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| NE555DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| NE555DRG4 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| NE555DRG4 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| NE555PSR | SO | PS | 8 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| NE555PWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SA555DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SA555DRG4 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SE555DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SE555DRG4 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| NA555DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| NA555DR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| NE555DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| NE555DRG4 | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| NE555DRG4 | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| NE555PSR | SO | PS | 8 | 2000 | 367.0 | 367.0 | 38.0 |
| NE555PWR | TSSOP | PW | 8 | 2000 | 367.0 | 367.0 | 35.0 |
| SA555DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| SA555DRG4 | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| SE555DR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| SE555DRG4 | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

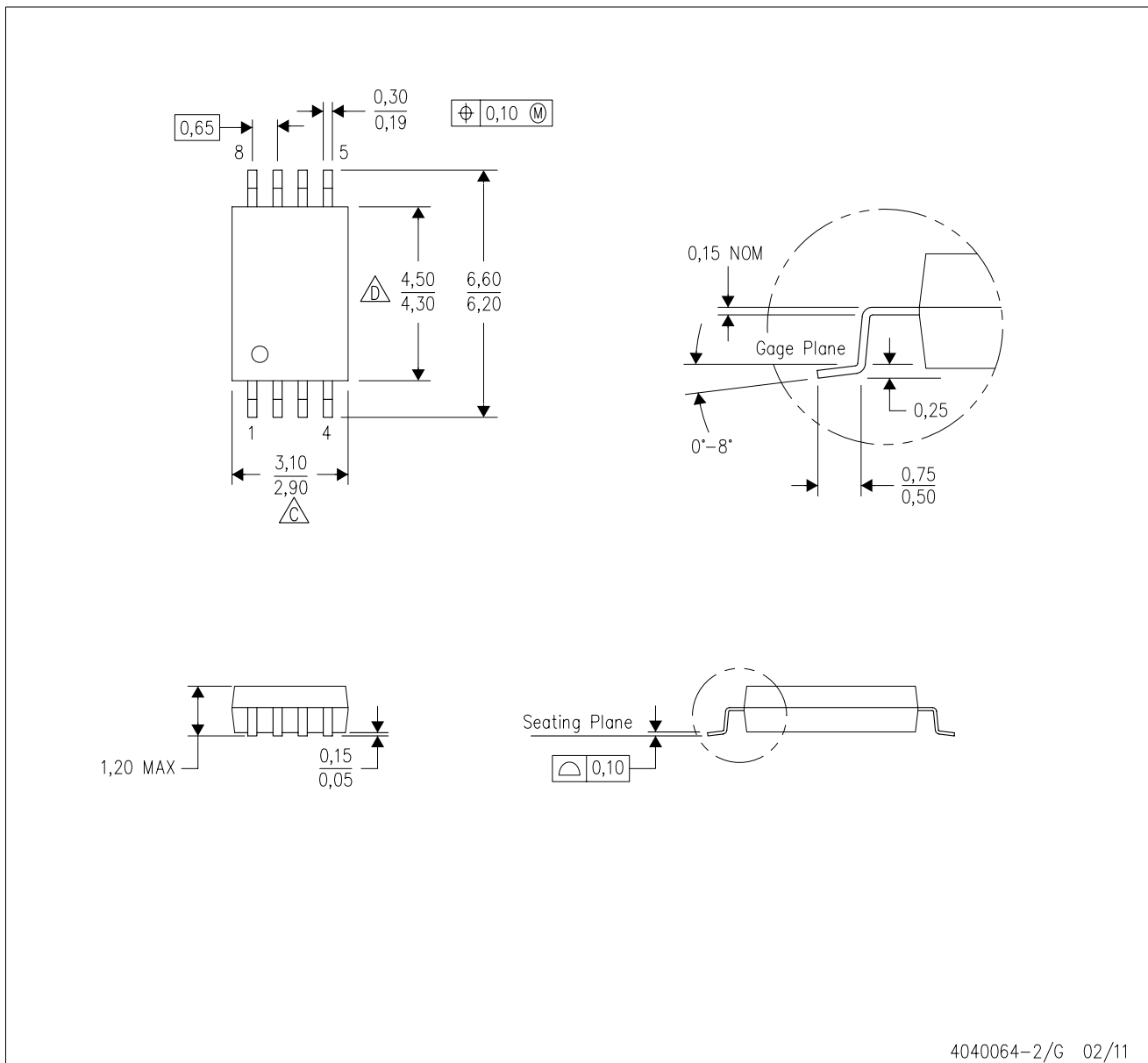
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040064-2/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

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