DIGITAL TECHNICS

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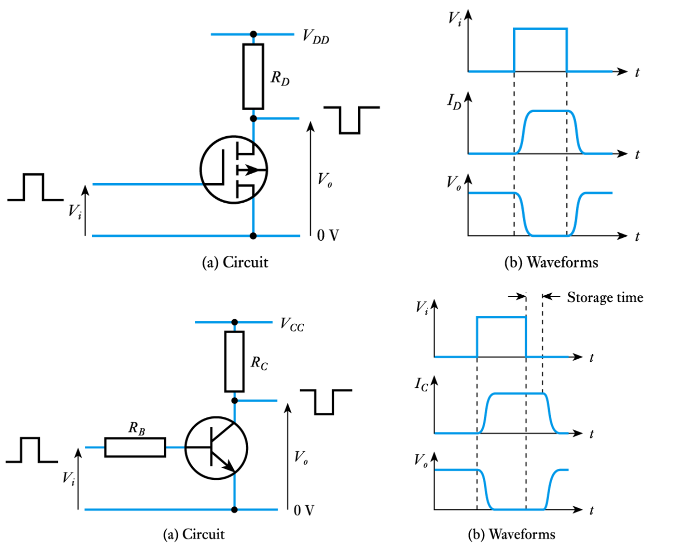
8. LECTURE: LOGIG CIRCUITS I: THE INVERTER. MOS DIGITAL CIRCUITS I

1st (Autumn) term 2018/2019

8. LECTURE: THE INVERTER. MOS DIGITAL CIRCUITS I.

1. The inverter: properties and functions
2. The MOS system, basic properties
3. MOSFET and basic MOS circuits
4. The CMOS concept, CMOS logic circuits

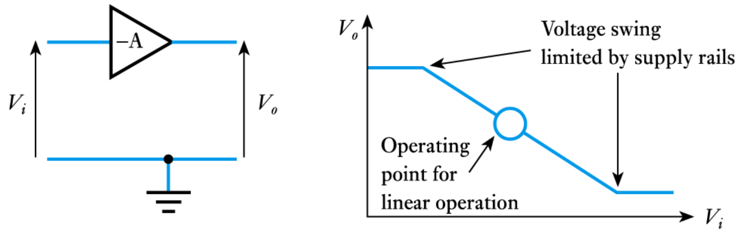
FET AND BJT AS A LOGICAL SWITCH



TRANSISTORS AS SWITCHES

– both FETs and bipolar transistors make good switches
– neither form produce *ideal* switches and their characteristics are slightly different
– both forms of device take a finite time to switch and this produces a slight delay in the operation of the gate
– this is termed the **propagation delay** of the circuit

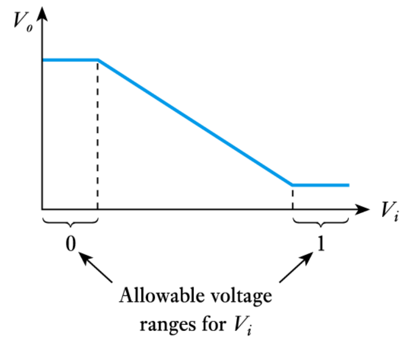
THE INVERTER: GATE CHARACTERISTICS



(a) Circuit symbol (b) Characteristic

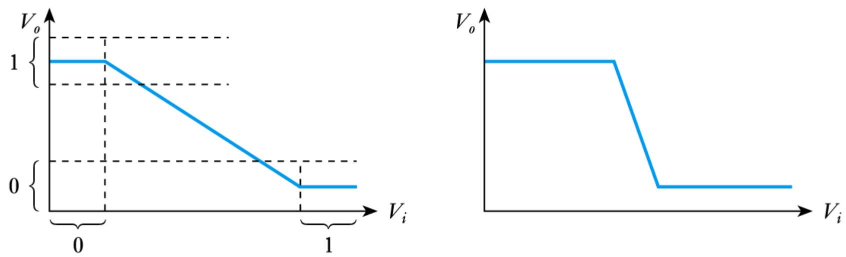
Consider the characteristics of a simple inverting amplifier we normally use only the **linear region**

We can use an inverting amplifier as a logical inverter but using only the **non-linear** region



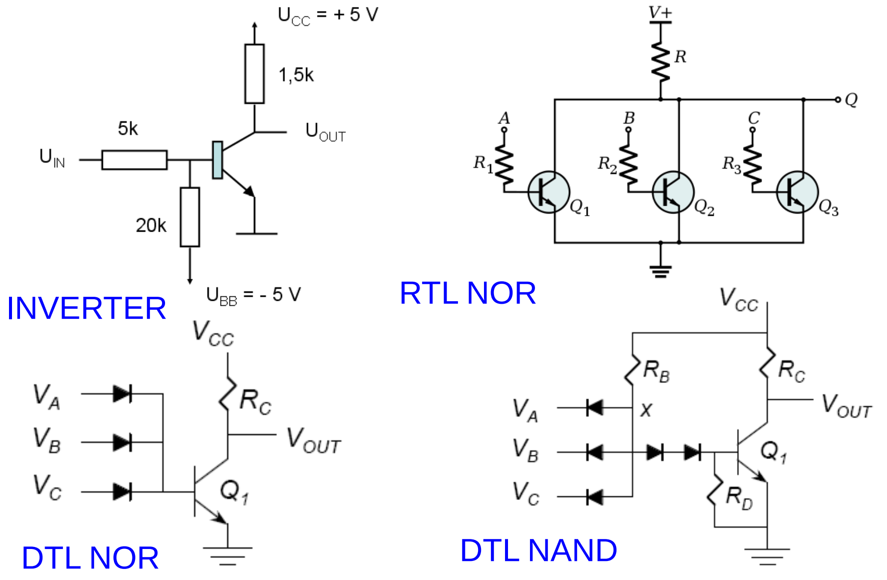
GATE CHARACTERISTICS

- we choose input values to ensure that we are always outside of the linear region – as in (a)
- unlike linear amplifiers, we use circuits with a rapid transition between the non-linear regions – as in (b)



(a) (b)

FROM SIMPLE INVERTER TO DTL GATES



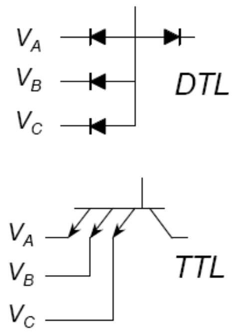
CONCEPTUAL STRUCTURE OF LOGIC GATES

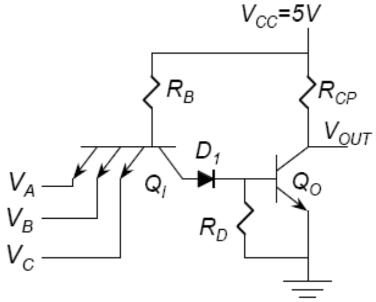
Input lines

Output lines

Generic circuit layout of digital gates

FROM DTL TO TTL ARCHITECTURE





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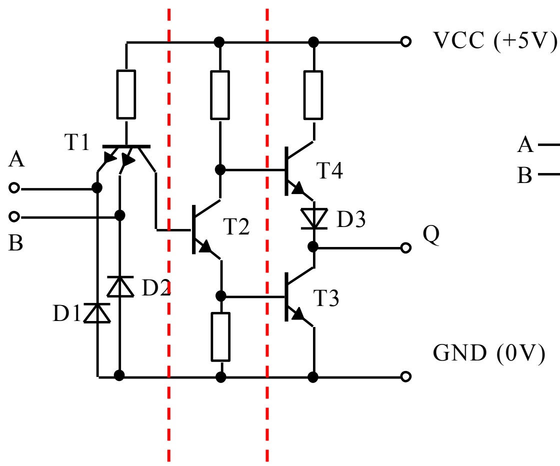
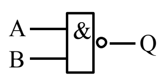
(BASIC/STANDARD) TTL GATE (NAND)





Combiner restorer buffer/driver

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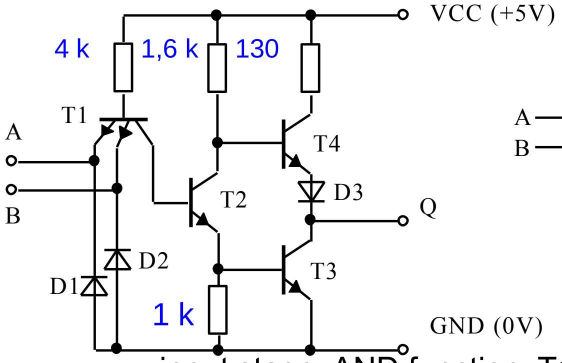
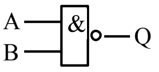
(BASIC/STANDARD) TTL GATE (NAND)





- input stage, AND function, T1,
- second stage, phase splitter, T2,
- output inverter stage with active pull-up, “totem-pole”, T3, T4, with diode level shifter, D3.
- Input diodes would be enough for the logic function, the transistor effect speeds up the switching.

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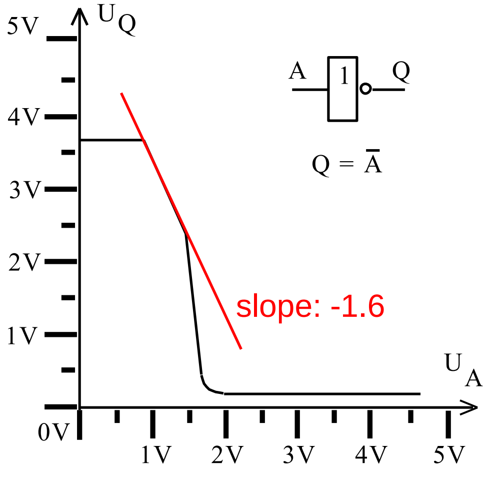
STANDARD TTL INVERTER TRANSFER CHARACTERISTICS



The shape of transfer characterisitcs is determined by the active pull-up and the totem-pole output.

In the 0.7-1.4 V input voltage region T2 transistor operates as a common emitter amplifier:

A_u = - 1.6 k / 1 k = -1.6

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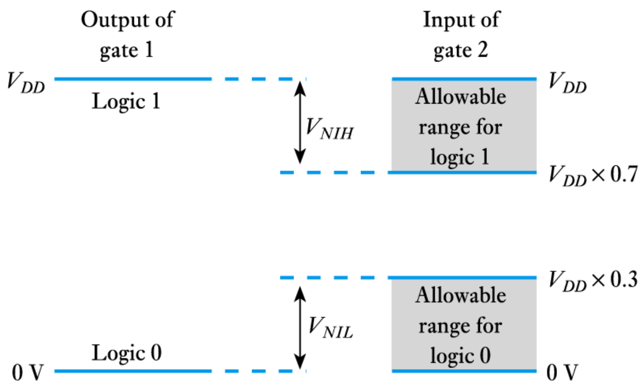
LOGIC LEVELS

- the voltage ranges representing ‘0’ and ‘1’ represent the **logic levels** of the circuit
- often **logic 0** is represented by a voltage close to 0 V but the allowable voltage range varies considerably
- the voltage used to represent **logic 1** also varies greatly. In some circuits it might be 2-4 V or even less, while in others it might be 12-15 V. In modern micoprocessors the voltage levels can be as low as about 1 V.
- in order for one gate to work with another the logic levels must be compatible

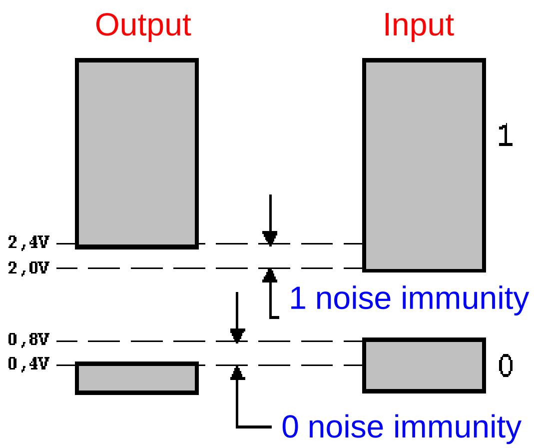
NOISE IMMUNITY

- noise is present in all real systems
- this adds random fluctuations to voltages representing logic levels
- to cope with noise, the voltage ranges defining the logic levels are more tightly constrained at the output of a gate than at the input
- thus small amounts of noise will not affect the circuit
- the maximum noise voltage that can be tolerated by a circuit is termed its **noise immunity**, U_{NI}

CMOS LOGIC LEVELS AND NOISE IMMUNITY



TTL LOGIC LEVELS AND NOISE IMMUNITY



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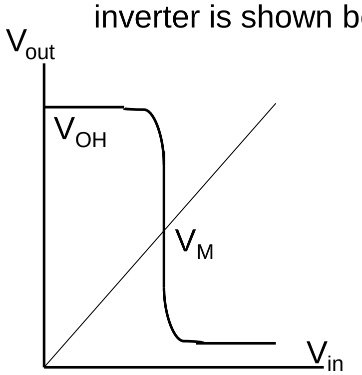
LOGIC INVERSION

- Most digital circuits use inverters: output of device is the opposite to the input. e.g. a logic input of 1, produces an output 0.
- The voltage-transfer characteristic (VTC) of an ideal inverter is shown below.



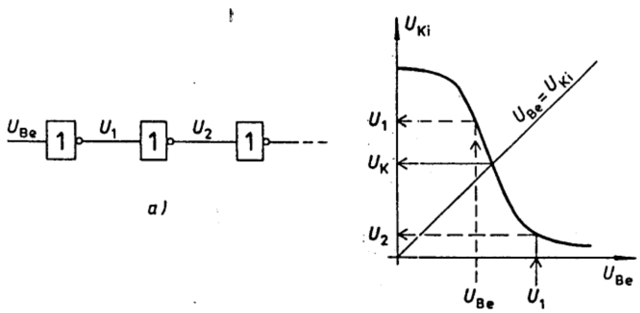
The straight line is the $V_{out} = V_{in}$

$V_{in} = 0$ V ➔ low, logic 0
$V_{in} = 5$ V ➔ high, logic 1

Actually we can have a range of voltages for V_{in} .

FUNCTIONS OF INVERTERS

- Signal restoring – active region of transfer characteristics, gain/amplification
- Noise rejection – small slope regions of the transfer characteristics



If the transfer characteristics is steep, the inverters (e.g. series connection) restore the digital signal levels.

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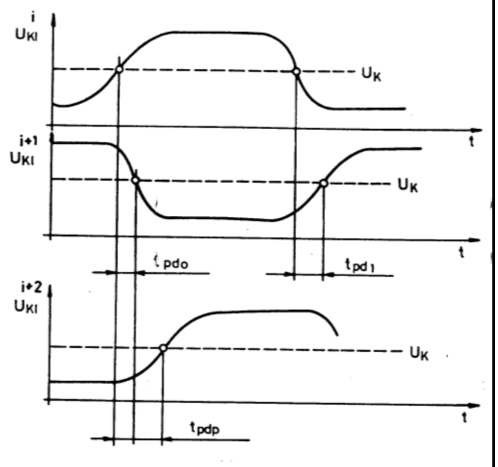
PROPAGATION DELAY

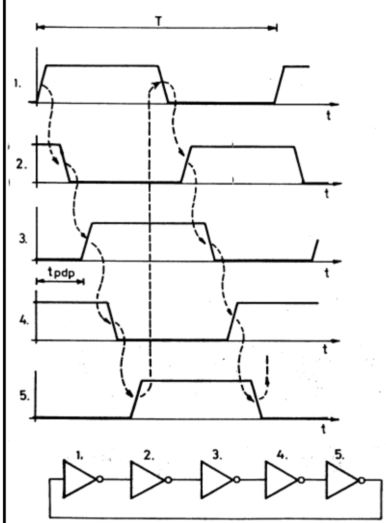
Propagation delay
Time elapsed between the appearance of input and output signal. It is different for up- and downgoing signal.

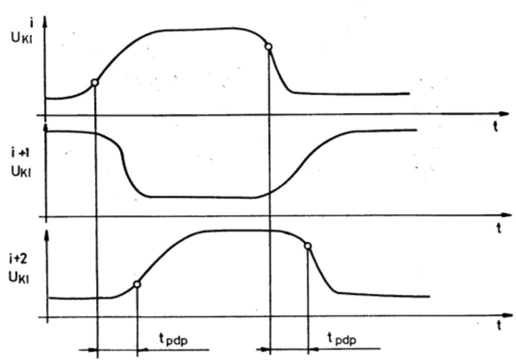
Pair propagation delay
In a long inverter chain (e.g.ring-oscillator) the signal shapes of every second inverter are the same. This defines the pair propagation delay.



RING OSCILLATOR

Ring oscillator: odd number of inverters.
The oscillation period: $T=Nt_{pdp}$





Signal shapes in an N = 5 ring oscillator.

IDEAL INVERTER

For a gate to be robust and insensitive to noise disturbances it is important that the ‘0’ and ‘1’ regions be as far apart as possible.

Some of the properties of the ideal digital gate

has the following properties
infinite gain in the transition region with the threshold voltage in the middle of the logic swing,

with high and low margins equal to half the swing,

the input and output impedance (resistance) are infinity and zero.

POWER DISSIPATION

Power is the product of current by voltage and is dissipated within a digital IC during switching.

The static dissipation is equal to the product of the dc voltage and the mean current taken from the supply.

$$P_{static} = I\,V = V_{DD}^2/R$$

For bipolar devices the power dissipated at the maximum frequency is usually about 20% greater that the static dissipation.

By contrast in a CMOS device the power dissipated is very small - this is one of the main advantages of CMOS over TTL based devices.

POWER DISSIPATION

The dynamic dissipation increases linearly with increase in clock frequency - we will investigate the reason for this later in the course.

$$P_{dynamic} = f\, C\, V_{DD}^2$$

The control of capacitance is also important.

SUMMARY OF THE IDEAL INVERTER

The ideal inverter should exhibit the following properties

Sharp switching with voltage when $V_{in} = V_{DD}/2$

Switching should be symmetric in voltage with equal noise margins.

Voltage should swing from 0 to V_{DD} (rail-to-rail switching)

Fast operation in time (no delay) and symmetric $0 \rightarrow 1$ and $1 \rightarrow 0$.

Low power dissipation during switching and no power dissipation when static.

And from a design and cost perspective should also be small

LOGIC FAMILIES

- Different devices use different voltages ranges for their logic levels
- They also differ in other characteristics
- In order to assure correct operation when gates are interconnected they are normally produced in families
- The most widely used families are:
  - **complementary metal oxide semiconductor (CMOS)**
  - **transistor-transistor logic (TTL)**
  - **emitter-coupled logic (ECL)**

LOGIC FAMILIES

Logic family: homogeneous circutis and networks with common unified proerties:

same supply voltage

same logic levels

similar propagation delays

same technology (usually on one chip)

LOGIC FAMILY CHARACTERISTICS

- **Complementary metal oxide semiconductor (CMOS)**
  - most widely used family for large-scale devices
  - combines high speed with low power consumption
  - in the past operated from a single supply of 5 – 15 V
  - excellent noise immunity of about 30% of supply voltage
  - can be connected to a large number of gates (about 50)
  - many forms – some with t_{PD} down to 1 ns
  - power consumption depends on speed (perhaps 1 mW)
  - V_{DD} has decreased in modern processes, high V_{DD} would damage modern tiny transistors, lover V_{DD} saves power
  - V_{DD} = 3.3, 2,5, 1.8, 1,5, 1.2, 1,0, …

LOGIC FAMILY CHARACTERISTICS

- **Transistor-transistor logic (TTL)**
  - based on bipolar transistors
  - one of the most widely used families for small- and medium-scale devices – rarely used for VLSI
  - typically operated from 5V supply
  - typical noise immunity about 1 – 1.6 V
  - many forms, some optimised for speed, power, etc.
  - high speed versions comparable to CMOS (~ 1.5 ns)
  - low-power versions down to about 1 mW/gate

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A COMPARISON OF LOGIC FAMILIES

Parameter	**CMOS**	**TTL**	**ECL**
Basic gate	NAND/NOR	NAND	OR/NOR
Fan-out	>50	10	25
Power per gate (mW)	1 @ 1 MHz	1 - 22	4 - 55
Noise immunity	Excellent	Good	Acceptable
t_{PD} (ns)	1 - 200	1.5 – 33	1 - 4

INTRODUCTION TO THE MOS TRANSISTOR

The invention of the transistor action (electrical signal amplification) in semiconducting material was a monumental accomplishment that has revolutionized the world. As with many inventions, the structure of the original invention has not only evolved, but also led to new structures. The first demonstration of transistor action (*Bardeen*, *Brattain*), the original point-contact transistor, was soon followed by the invention of the junction bipolar transistor (*Shockley*). This second structure is viewed as the basis of modern microelectronics, because it laid the foundation for the concept of building an entire electrical circuit on a single piece of semiconducting material (*Kilby*, *Noyce*).

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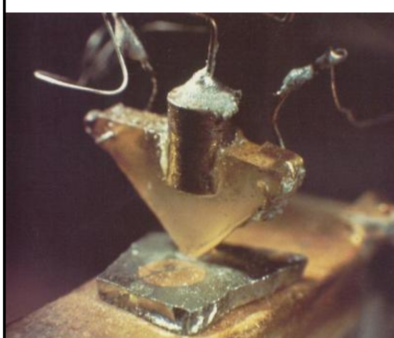

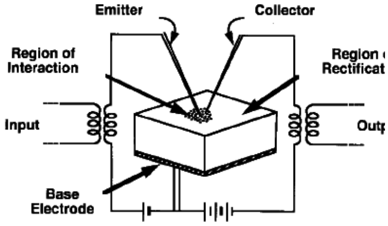

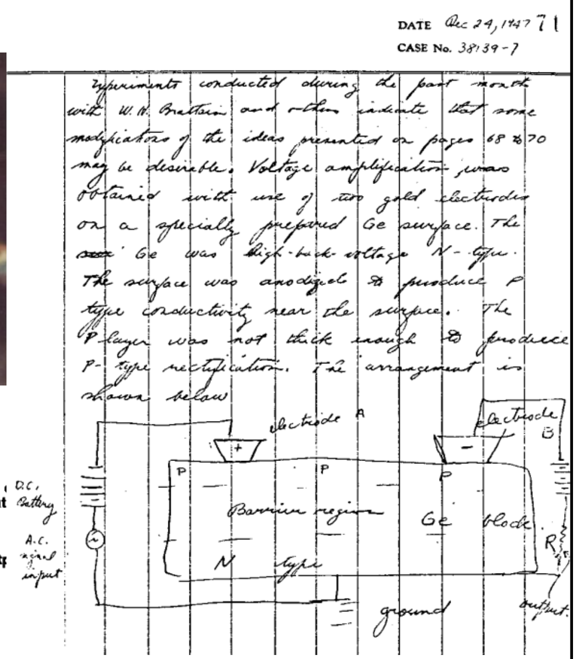

DATE Dec 24, 1947 71
CASE No. 38139-7

Experiments conducted during the past month with W. H. Brattain and others indicate that some modifications of the ideas presented on pages 68 & 70 may be desirable. Voltage amplification was obtained with use of two gold electrodes on a specially prepared Ge surface. The ~~sur~~ Ge was high-back-voltage N-type. The surface was anodized to produce P type conductivity near the surface. The P-layer was not thick enough to produce P-type rectification. The arrangement is shown below

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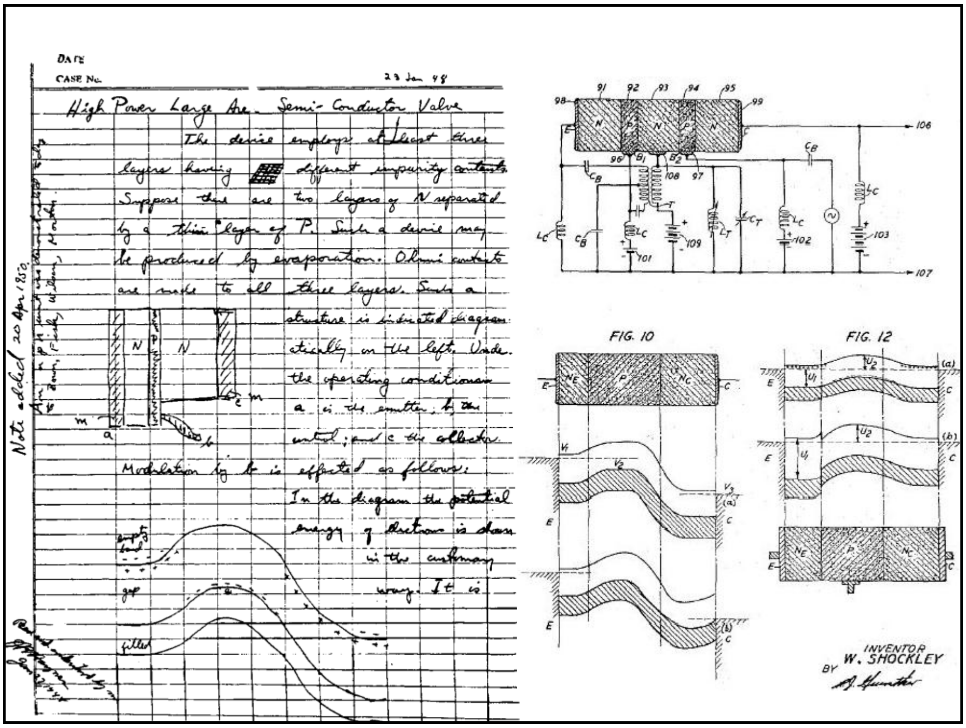
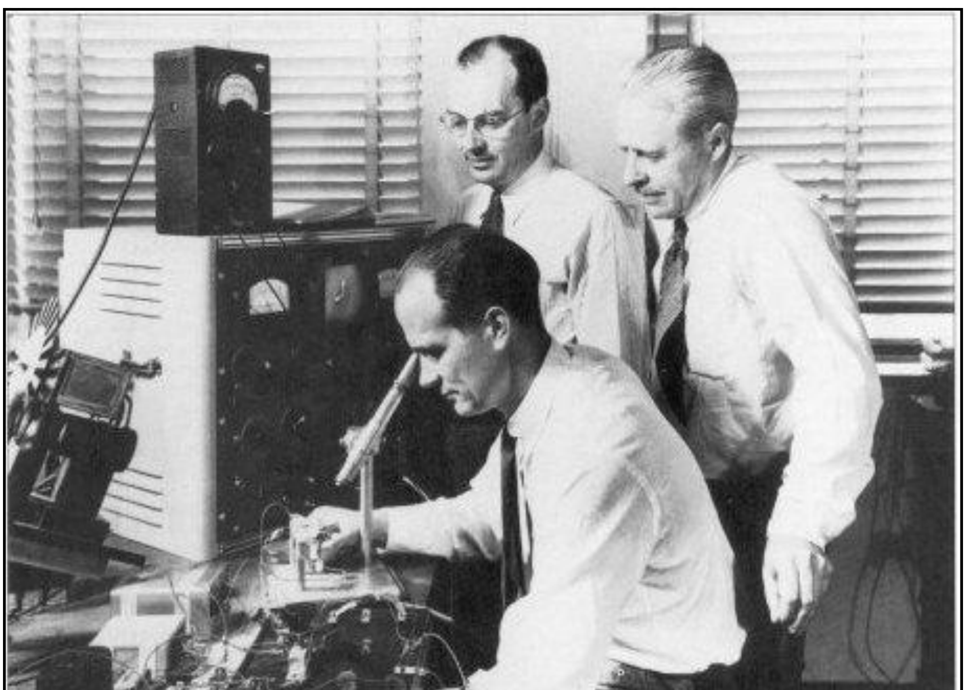
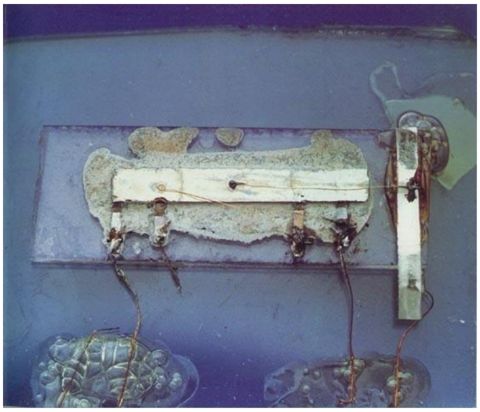
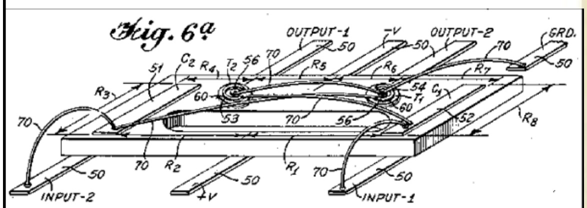
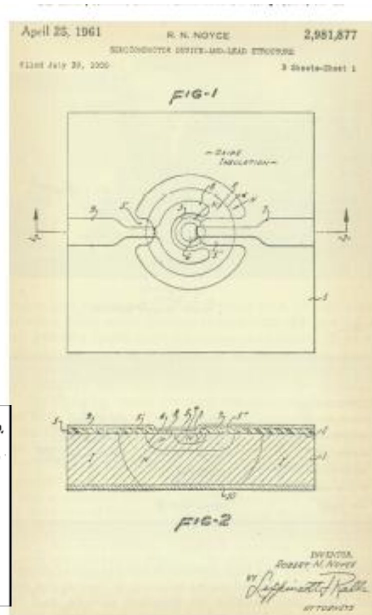

DATE
CASE No.
23 Jan 48
High Power Large Area Semi-Conductor Valve
The device employs at least three layers having different impurity contents. Suppose there are two layers of N separated by a thin layer of P. Such a device may be produced by evaporation. Ohmic contacts are made to all three layers. Such a structure is indicated diagrammatically on the left. Under the operating conditions a is the emitter, b the control; and c the collector.
Modulation by b is effected as follows: In the diagram the potential energy of electrons is shown in the customary way. It is
Note added 20 Apr 1950
FIG. 10
FIG. 12
INVENTOR
W. SHOCKLEY
BY









INTRODUCTION TO THE MOS TRANSISTOR

It is interesting to recognize, however, that the junction bipolar transistor and the technology that was developed to fabricate it led to another type of transistor, the metal-oxide-semiconductor (MOS) transistor. Both the theory of MOS transistor operation and the technology associated with its fabrication were derived from the classic junction bipolar structure and related research. Today, however, the MOS transistor is the structure primarily used in the continuing exponential growth of microelectronics (Moore’s law).

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THE MOSFET

The MOSFET has proven to be the device par excellence for integrated circuit logic because of its relative simplicity (compared to bipolar transistors), small size, and low power demands (in large part because of its infinite input resistance); only in the area of speed does MOSFET logic circuitry fall short of bipolar logic circuitry.

In the followings we will look at several MOSFET logic families. They are all basically common-source circuits and differ only in the nature of their load devices.

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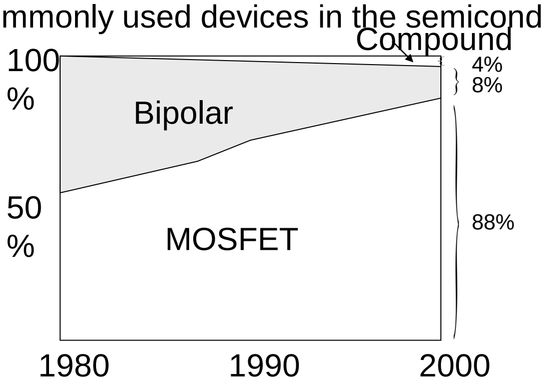
THE MOS TRANSISTOR

- Metal-oxide-semiconductor
- Also called MOSFET (MOS Field Effect Transistor)
- Simple, symmetric structure
- Switch, good for digital, logic circuit
- Most commonly used devices in the semiconductor industry



Market of semiconductor products

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FET AND MOSFET

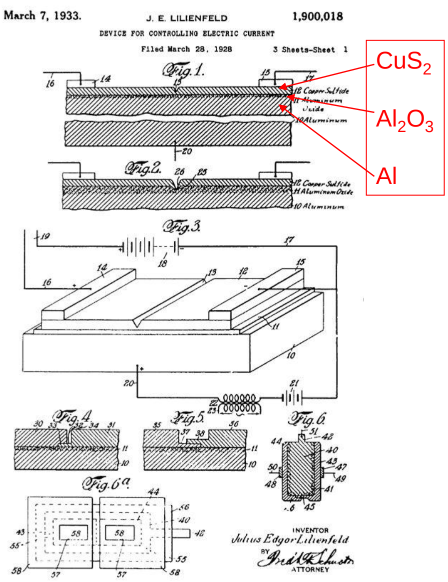
FET – Field Effect Transistor

The metal-oxide-semiconductor field-effect transistor (MOSFET) is the most important device for very-large-scale integrated circuits such as microprocessors and semiconductor memories.

Voltage applied to insulated gate controls current between source and drain. Low power allows very high integration.

The principle of the surface field-effect transistor was first proposed in the 1930s by Lilienfeld (US patent) and Heil (British patent).

THE (HISTORIC) FET PATENT



A page from the original patent by J. Lilienfeld

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Filed: March 28, 1928
Published: March 7, 1933
1900018

In today's concepts:
Depletion type p-channel MOSFET

J. LILIENFELD AND THE FET

Julius Edgar Lilienfeld (1882-1963) was a physicist of Polish origin. He was born in Lemberg, Galicia, in the Austrian-Hungarian Monarchy (now called Lviv in Ukraine), moved to the United States in the early 1920s.

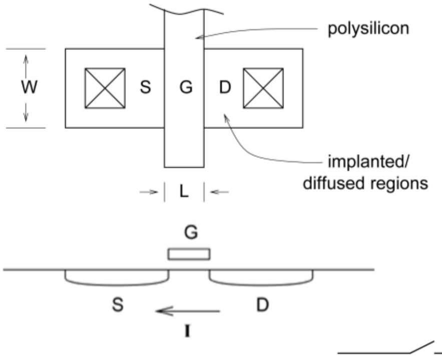
Lilienfeld is credited with the first patents on the field effect transistor (1920s) and electrolytic capacitor (1931).

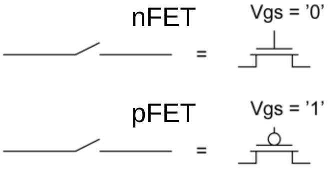
He filed several patents describing the construction and operation of transistors as well as many features of modern transistors. (US patent #1,745,175 for an FET-like transistor was granted January 28, 1930.) When Brattain, Bardeen, the future Nobelist, and Robert Gidney tried to get patents on their earliest devices, most of their claims were rejected due to the Lilienfeld patents.

MOSFET

Top view

Cross section





The gate acts like a capacitor. A high voltage on the gate attracts charge into the channel. If a voltage exists between the source and drain a current will flow. In its simplest approximation the device acts like a switch.

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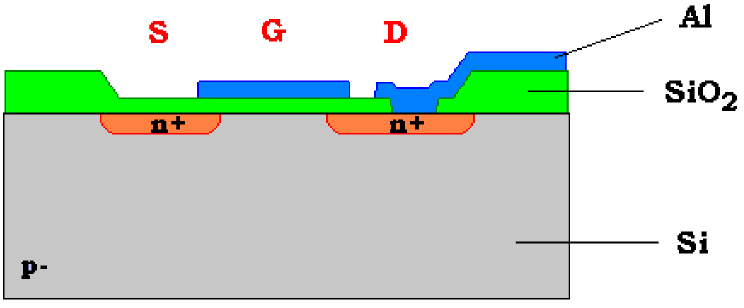
MOS TRANSISTOR



Early MOS transistor, metal-gate , diffused contacts.

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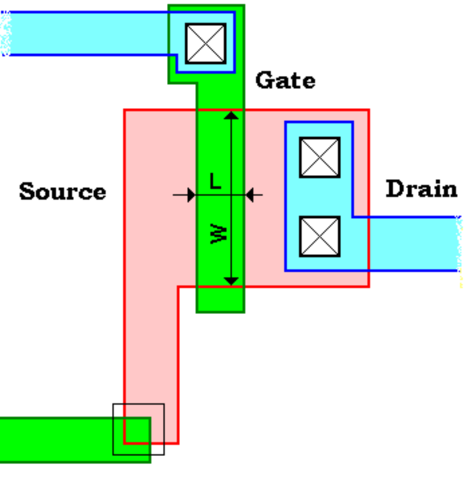
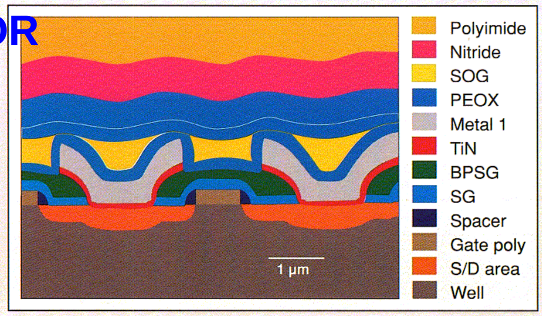
MOS TRANSISTOR

Self-aligning, poly-silicon gate

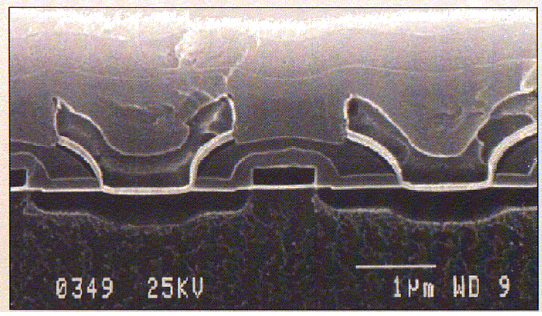


MOS TRANSISTOR STRUCTURE

Sub-micrometer transistor structure

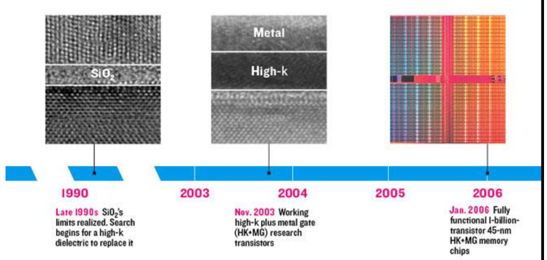


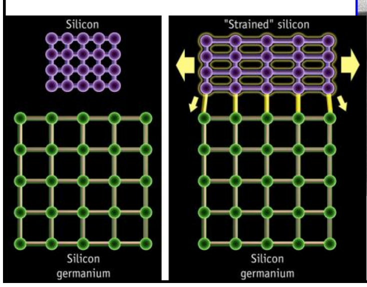
0.8 µm CMOS transistor cross-section

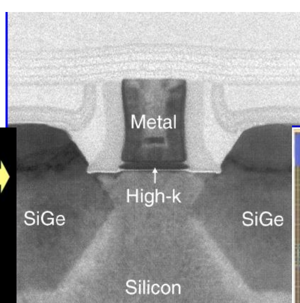


THE 45 nm TECHNOLOGY

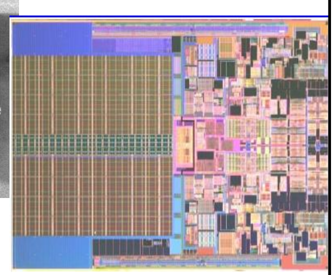
- High diel. const. HfO_2 based gate insulator in place of SiO_2
- Metal gate in place of poly-Si
- Strained Si structure (SiGe)



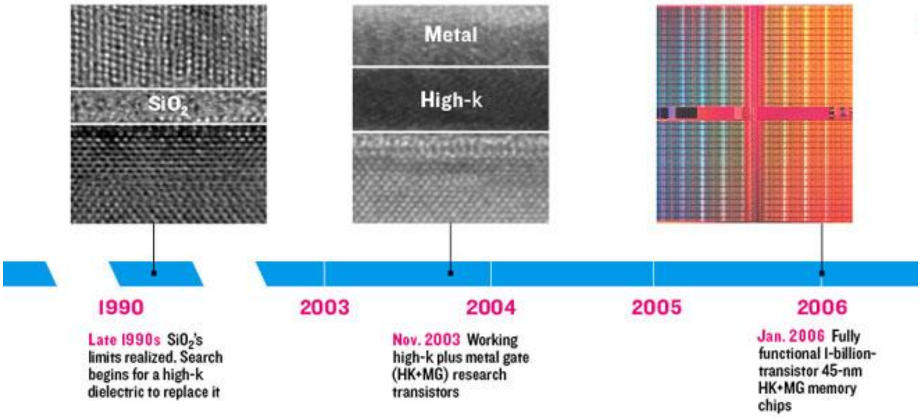




Dual core



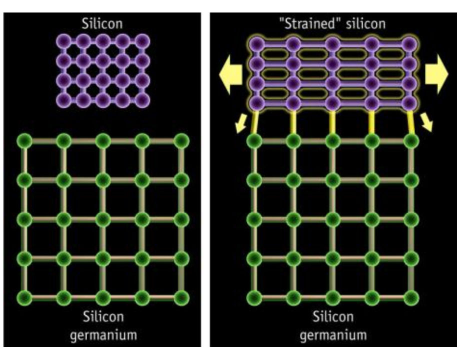
THE MOSFET TODAY: THE 45 nm TECHNOLOGY

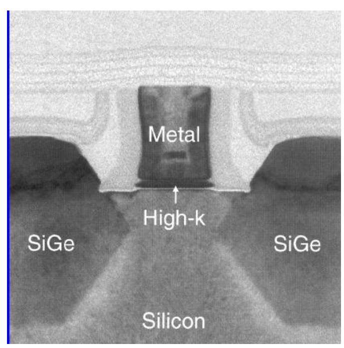


THE IC TODAY: THE 45 nm TECHNOLOGY

The 45 nm technology:

High diel. const. HfO_2 based gate insulator in place of SiO_2
Metal gate in place of poly-Si
Strained Si structure (SiGe)



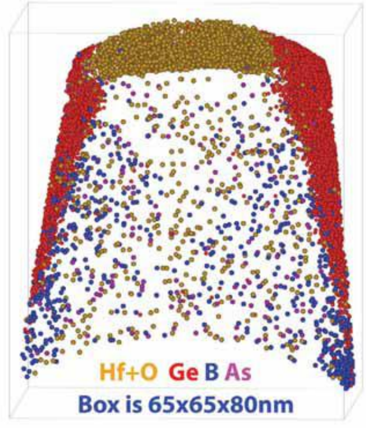


THE IC TODAY: THE 45 nm TECHNOLOGY

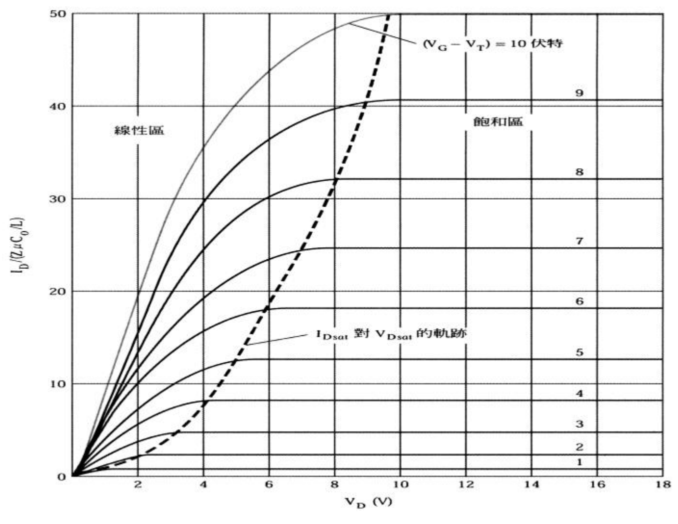
Atom probe tomography

The solute distributions across a 32 nm technology nFET transistor extracted by a focused ion beam-based technique from a commercial Intel® i5-650 microprocessor is shown in an atom map in fig.

The gate oxide was found to be 80 at. % Hf+O, 20 at. % Si, the source and drain regions either side of the channel region contained a maximum of 25 at. % Ge. The distributions of the B and As atoms are clearly shown in relationship to the source and drain regions.



MOSFET OUTPUT CHARACTERISTICS



MOS CHARACTERISTICS

The analytic form of the input (transfer) characteristics based on the elementary physical model is

$$I_{DS} = K\,(U_{GS} - U_T)^2$$

K - device constant (depends on the technology and geometry of the device

U_T - turn on or threshold voltage

The current through the device is

$$I_{DS} = K((U_{GS} - U_T) - U_{DS}/2)U_{DS}$$

MOSFET AS A SWITCH

The MOSFET can be considered in a very good approximation as an ideal switch.

When closed (cut-off) the resistance is greater than 10^{10}-10^{12} ohm.

When open the resistance is a few hundred ohms, this can be taken as a short circuit with respect to the cut-off state.

The switchover can be controlled practically without power.

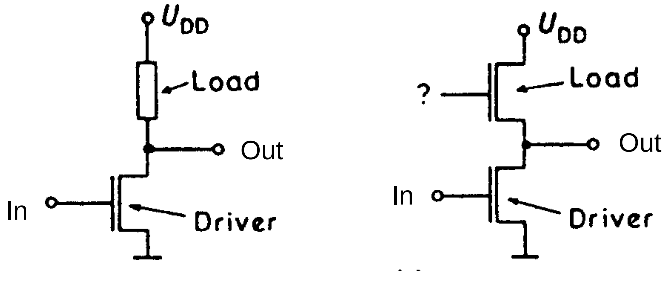
MOS CIRCUITS AND LOGIC GATES: BASIC PRINCIPLES

Basic circuit: inverter, both the control- (driver-) transistor and the load are active elements.

Inverter with passive loading: the load transistor is not controlled by the input. Its gate is connected to the supply voltage or to an other electrode of the transistor.

Inverter with active load: the loading transistor is also controlled by the input signal. In this case one of the transistors is of NMOS, the other is of PMOS type.

MOS INVERTERS



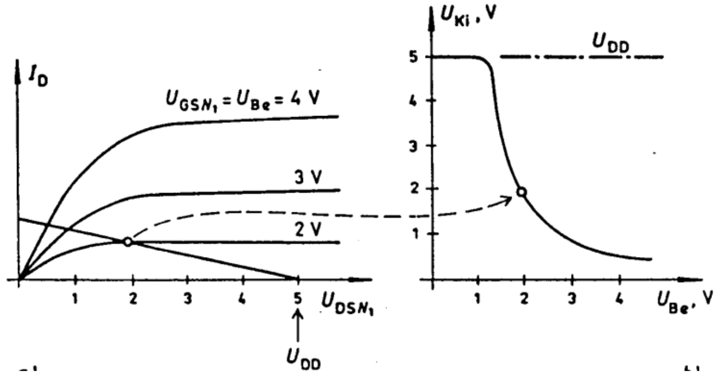
Resistor and FET loaded NMOS inverters

If U_{in} = 0 the driver transistor is cut-off, U_{out} = 1
If U_{in} = 1 the driver transistor is open/conducting, U_{out} = 1

Instead of resistor, a MOS transistor is used as a load (smaller area on the chip) . Depending on the connection of the load:

passive loaded inverter
active loaded inverter

RESISTOR LOADED INVERTER



As larger is the load resistor, as steeper is the transfer characteristics.
However it is difficult to implement large resistors in ICs.
Solution: MOS inverters.

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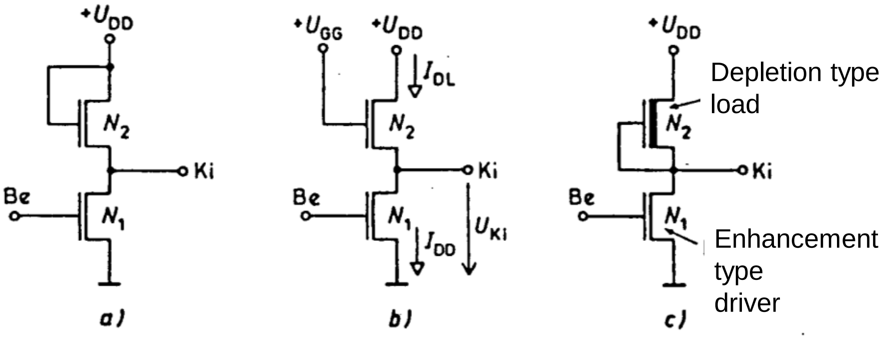
PASSIVE LOADED NMOS INVERTERS



NMOS inverters (drivers enhancement type), loads (a) enhancement, saturated, (b) enhancement, triode, (c) depletion type.
The load transistor is used as a passive, nonlinear two-port.

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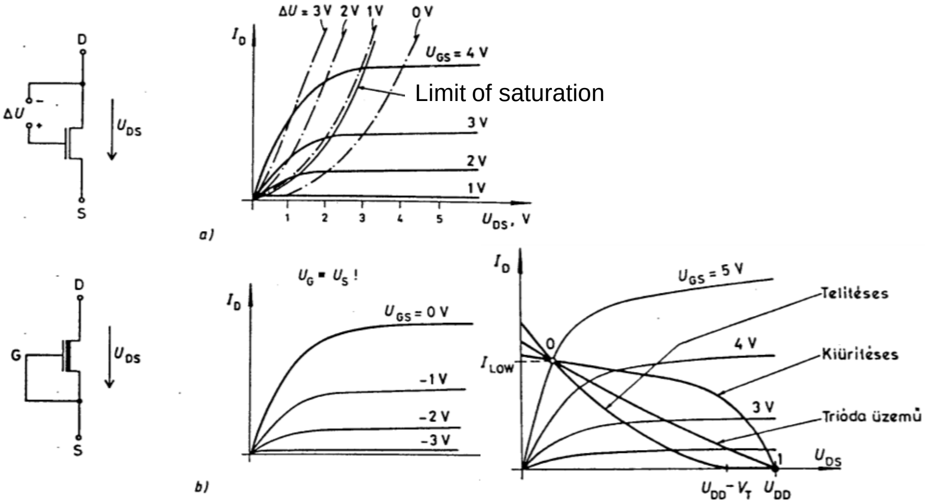
LOAD CHARACTERISTICS



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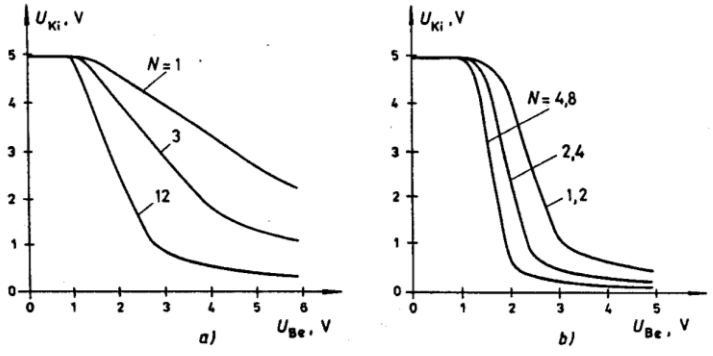
TRANSFER CHARACTERISTICS



NMOS inverters are ratio type circuits: the output LOW level is determined by the ratio of the channel resistance of the driver and the load transistors. The load transistor should exhibit large channel resistance, the driver should have low resistance. This can be set by appropriate (different) channel width-to-length (W/L) ratios.

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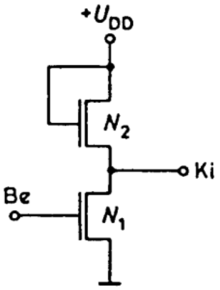
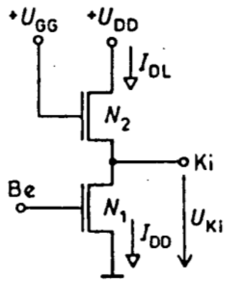
INVERTER PROPERTIES

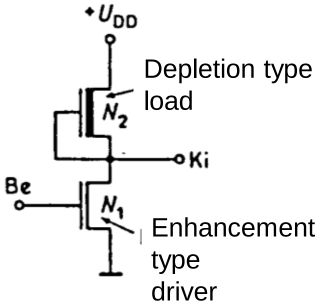


Output HIGH level $U_{DD} - U_{th}$
Output LOW level does NOT reach0 V
Power is dissipated when output LOW
Rise and fall times differ
Simple technology (only one transistor type)



Output LOW level does NOT reach 0 V
Power is dissipated when output LOW
Rise and fall times differ
Two power supplies (U_{DD} and U_{GG})
Simple technology (only one transistor type)

INVERTER PROPERTIES



Output LOW level does NOT reach 0 V
Power is dissipated when output LOW
Rise and fall times differ
Complicated technology (two transistor types)

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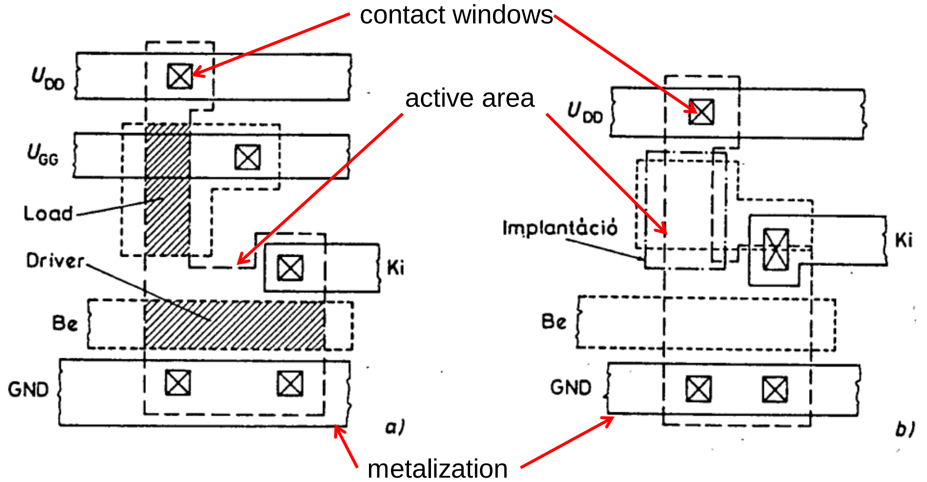
NMOS INVERTER TOPOLOGY



Topology of triode mode (a) and depletion mode load (b) inverters.

Dashed line – active area, dotted line – poly-silicon (gate)

ACTIVE LOAD CMOS INVERTER

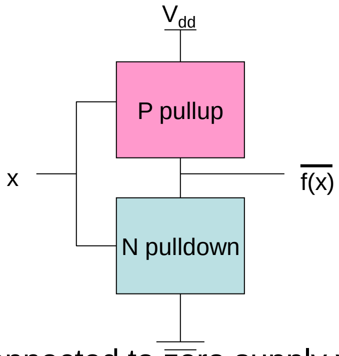
An extremely useful and important circuit for digital applications is a combination of n-channel and p-channel MOS transistors on adjacent region of the chip. A pair forms the basic *complementary MOS* (CMOS) inverter.
In this circuit the drains of the two transistors are connected together and form the output, while the input terminal is the common connection to the gates.
The circuit operates as an inverter – with HIGH at the input, the output is in the LOW state, whereas a LOW input produces HIGH output.
The beauty of this circuit is that one of the devices is turned for either condition. Since the devices are connected in series, no drain current flows except for a small charging current during the switching process from one state to the other.
Since the CMOS inverter uses ultra little power, it is particularly useful in applications such portable equipments.
CMOS is also advantageous in ULSI circuits, since even small power dissipation in each transistor becomes a problem when millions of them are integrated on a chip.

COMPLEMENTERY MOS: CMOS

n-channel and p-channnel MOS transistor pairs

PMOS

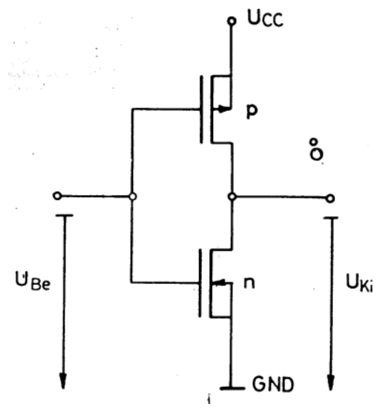
drain connected to high (+) supply voltage
pulls-up the output voltage if input is 0 (low).

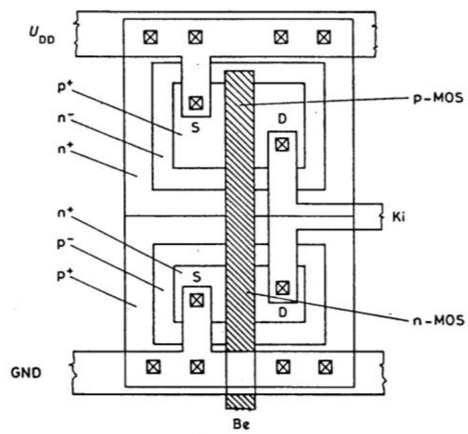


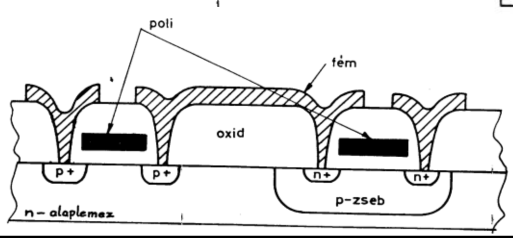
NMOS

source connected to zero supply voltage (GND)
pulls-down the output voltage if input is 1 (high).

ACTIVE LOAD CMOS INVERTER







A possible topology and a possible cross section of the CMOS inverter

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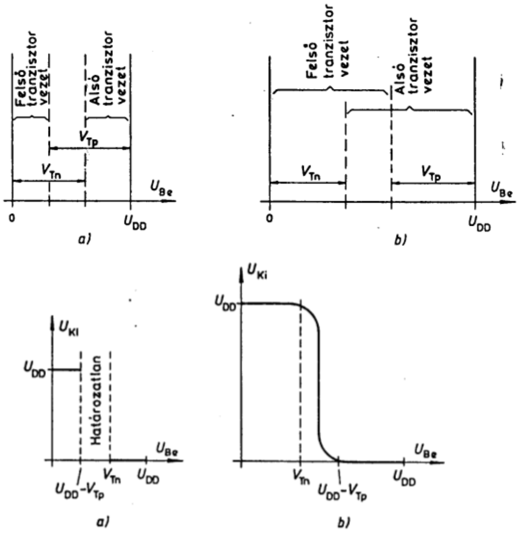
CMOS: THRESHOLD- AND SUPPLY-VOLTAGES



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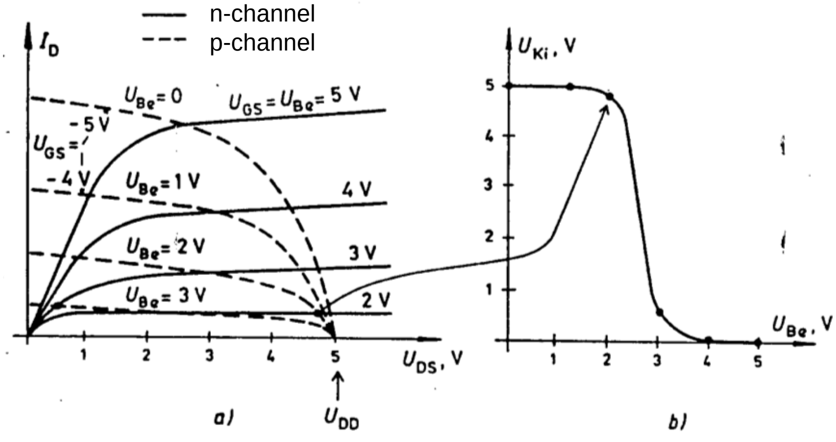
CMOS INVERTER TRANSFER CHARACTERISTICS



Construction of CMOS inverter transfer characteristics

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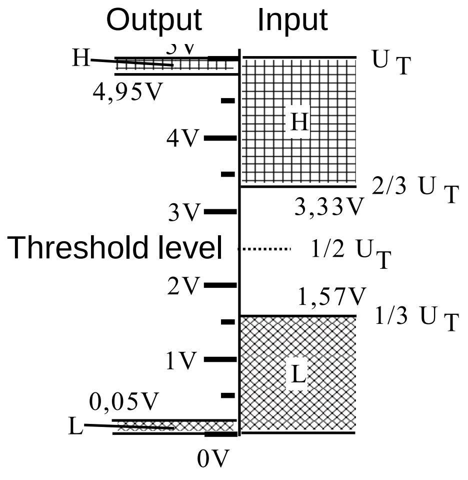
CMOS LOGIC CITCUITS: MAIN FEATURES

- MOSFET occupies the smallest area on the Si wafer
- MOSFET can be fabricated with less number of steps
- MOSFET is controlled with practically zero power
- In stationary state it does not draw current from the supply
- Supply voltage can vary in a wide range
- No resistors are necessary

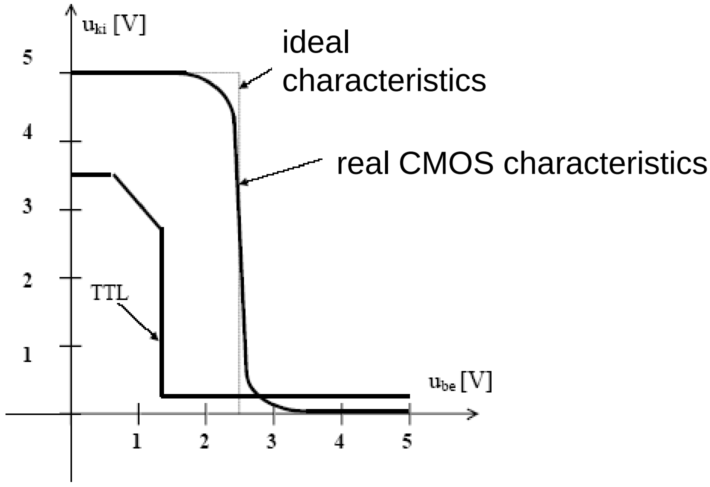
CMOS LOGIC VOLTAGE LEVELS (SSI MODULAR LOGIC)



CMOS logic voltage levels with +5 V supply voltage.

Can operate with supply from +3 to +15 V.

(SSI MODULAR) CMOS INVERTER: TRANSFER CHARACTERISTICS



CMOS INVERTER CAPACITANCES

Inverter input capacitance:

$$C_{be}=C_{GSn}+C_{GBn}+C_{GSp}+C_{GBp}+2(C_{GDn}+C_{GDp})$$

Inverter output capacitance

$$C_{ki}=C_{DBn}+C_{DBp}+2(C_{GDn}+C_{GDp})$$

C_{GS} - gate-source
C_{GB} - gate-substrate
C_{GD} - gate-drain
C_{DB} - drain-substrate

RISE- AND FALL TIMES

In a CMOS transistor pair the rise and fall times are equal:

$$t_{fl} = \frac{C_L}{\beta(U_{DD} - U_T)}\left[2\frac{U_T - 0{,}1U_{DD}}{U_{DD} - U_T} + \ln(19 - 20\frac{U_T}{U_{DD}})\right]$$

CL is the load capacitance: i.e. sum of the output capacitance of the inverter, of the input capacitance of the loading circuit, and of the capacitance of interconnections.

For a given technology (gate length L) wider transistors (β is proportional to W) and higher supply voltage (U_{DD}) give shorter switching times, while for higher capacitive loads (C_L) it increases.

Therefore using wider transistors compensate for higher capacitive loads in the circuit.

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CMOS ENERGY AND POWER EQUATIONS

$$E = C_L V_{DD}^2 P_{0\to 1} + t_{sc} V_{DD} I_{peak} P_{0/1\to 1/0} + V_{DD} I_{leak}$$

$$f = P * f_{clock}$$

$$P = C_L V_{DD}^2 f + t_{sc} V_{DD} I_{peak} f + V_{DD} I_{leak}$$

Dynamic power (~80% today and decreasing relatively)

Short-circuit power (~5% today and decreasing absolutely)

Leakage power (~15% today and increasing)

REVISION QUESTIONS

1. Define the concept of logic family.

2. Explain the governing parameters of the logic families.

3. Describe the difference between the bipolar integrated circuits and MOS integrated circuits.

4. What is noise immunity? What is propagation delay?

5. Describe the characteristics of MOS logic.

6. Describe enhancement type MOS and depletion type MOS with constructional details.

END OF LECTURE

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