DIGITAL TECHNICS

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9. LECTURE (LOGIC CIRCUITS, PART 2): MOS AND CMOS DIGITAL CIRCUITS II

2nd (Autumn) term 2018/2019

2ND HOME ASSIGNMENT

Submission deadline:

Wednesday 28 November

Discussion possibility:

Wednesday 14 November
(10h-12h, C301)

2

9. LECTURE: MOS AND DIGITAL CIRCUITS II

1. NMOS gates, complex gates

2. CMOS gates, complex gates

3. NMOS and CMOS flip-flops

4. MOS functional circuits (memories, multiplexers, decoders, adders, etc.)

Recommended literature:
Mojzes I. (ed.): *Mikroelektronika és elektronikai technológia*

3

THE MOSFET AND CMOS INTEGRATED CIRCUITS

The Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) is the prevailing device in microprocessors and memory circuits.

The MOSFET's advantages over other types of devices are its (i) mature fabrication technology, (ii) its successful scaling characteristics and (iii) complementary MOSFETs yielding CMOS circuits.

The fabrication process of silicon devices has evolved over the last 50 years into a mature, reproducible and reliable integrated circuit manufacturing technology.

MOS GATES: PASSIVE LOADING

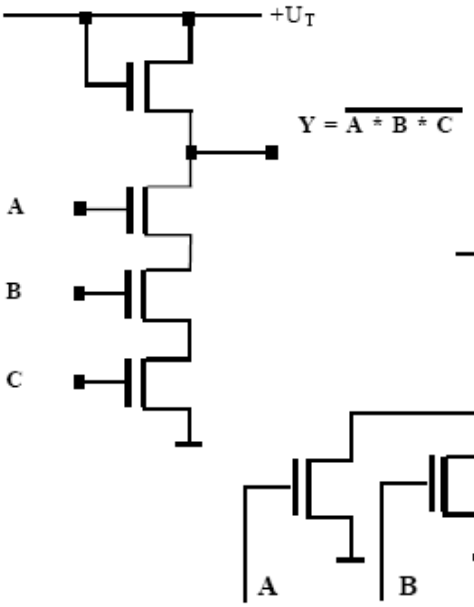
Gates are inverters in disguise.

Three-types of passive loaded inverters: three types of gates.

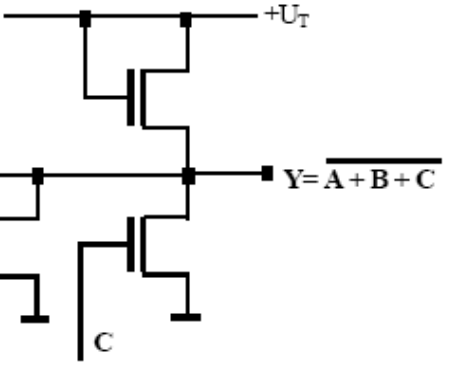
The nowadays mostly used *depletion-type* load variant will be discussed.

5

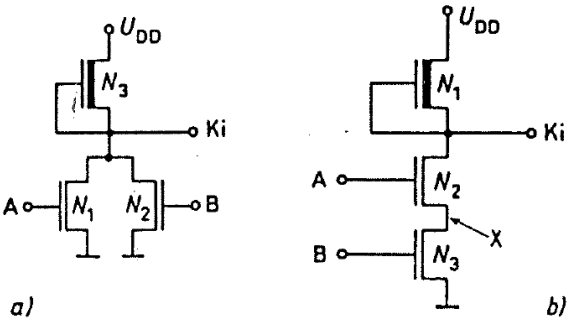
BASIC MOS CIRCUITS: NOR & NAND GATE



MOS circuits are simple. The control- (drive-) transistors determine the logic function. Even in the case of complex logic functions, one load transistor is sufficient.



NMOS GATES: NOR AND NAND

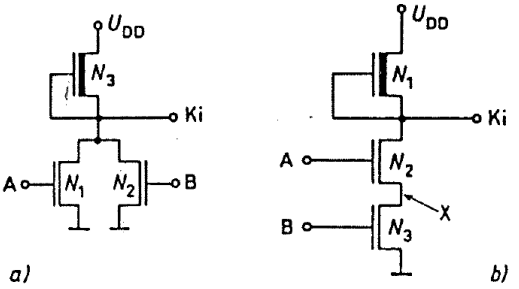


2-input NOR (a) and NAND (b) gates

NOR gate: the dimensions (length and width) of the driver gates are the same as in the inverter. If only one of them is open, the output LOW level and the time is also the same. If both driver inputs are HIGH, both parallel transistors will be open, and the above parameters will be improved.

7

NMOS GATES: NOR AND NAND



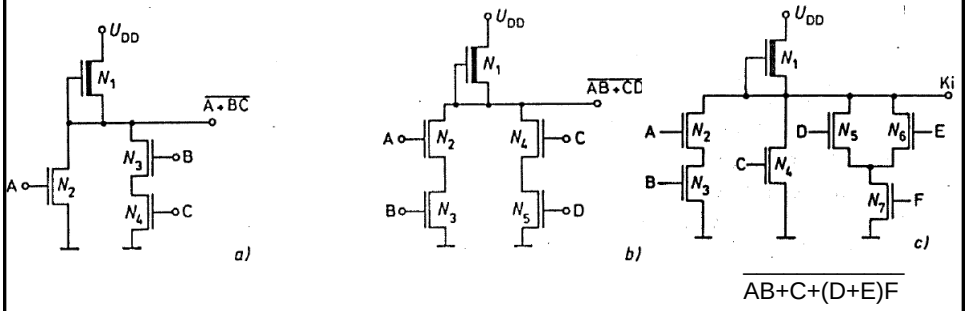
2-input NOR (a) and NAND (b) gates

NAND gate: For N inputs, the widths (W) of the driver transistors are N times wider, to ensure the same output LOW level and time as in the case of the inverter.
Usually at most four transistors are connected in series, because the too large dimensions result in too large capacitive loads, which will increase the propagation delay of the circuit.

8

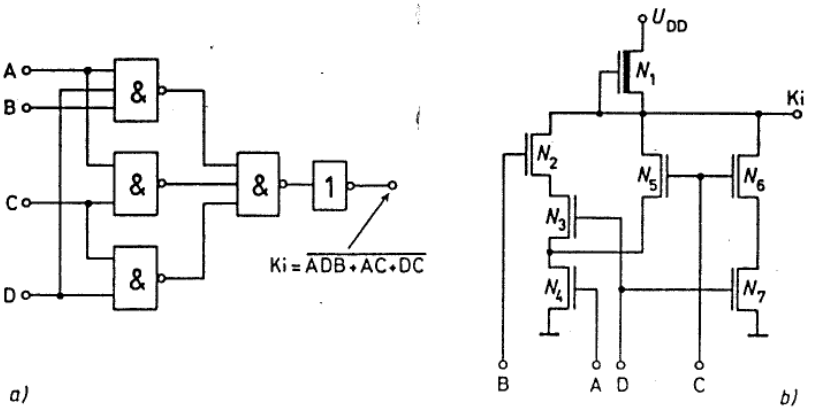
COMPLEX GATES

Various complex functions can easily be implemented using MOS circuits:



$\overline{AB+C+(D+E)F}$

COMPLEX GATES



The feasibility of complex gates offers new possibilities with respect to customary TTL circuit solutions. E.g. the TTL circuit consisting of five gates (a) can be implemented with a 7-transistor complex gate (b).
Advantages: (i) fewer components, (ii) faster operation (the complex gate is only one gate with one unit delay), while the TTL version represents 3 units of delay.

CMOS LOGIC CIRCUITS

CMOS technology uses both NMOS and PMOS transistors. The transistors are arranged in a structure formed by two complementary networks:

pull-up network is complement of pull-down;
parallel→series, series→parallel.

CMOS logic circuits may be considered switching circuits because of the extreme little control current necessary.

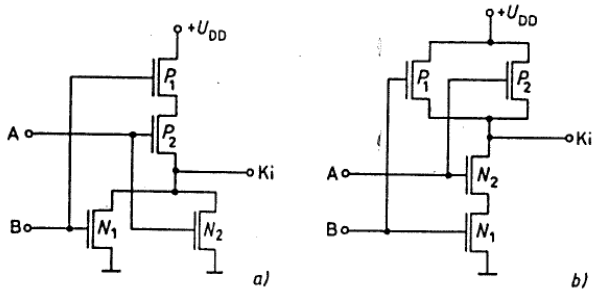
Most commonly used circuit in IC chip since 1980s.

Low power consumption.
High temperature stability.
High noise immunity.
Symmetric design.
Still dominates the IC market.
Backbone of information revolution.

CMOS LOGIC CITCUITS: MAIN FEATURES

- MOSFET occupies the smallest area on the Si wafer
- MOSFET can be fabricated with less number of steps
- MOSFET is controlled with practically zero power
- In stationary state it does not draw current from the supply
- Supply voltage can vary in a wide range
- No resistors are necessary

CMOS GATES: NOR AND NAND



2-input NOR (a) and NAND (b) gates

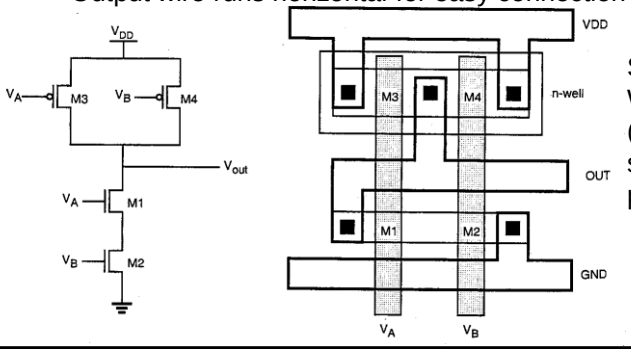
Advantages: it is NOT a ratio-circuit, it is not necessary to use differently sized transistors.
No static dissipation (either the lower or the upper branches are always in cut-off.
Disadvantages: uses more transistors than the NMOS implementation (for N inputs NMOS uses N+1, CMOS needs 2N transistors).

13

EXAMPLE: CMOS 2-NAND WITH LAYOUT

The CMOS 2-NAND circuit and an example layout are shown below.
Attractive layout features:

- Single polysilicon lines (for inputs) are run vertically across both N and P active regions
- Single active shapes are used for building both NMOS devices and both PMOS devices
- Power bussing is running horizontal across top and bottom of layout
- Output wire runs horizontal for easy connection to neighboring circuit



Substrate: p-type
$W_p = 2\ W_n$
(from current and switching consideration of p- and n-channel MOS

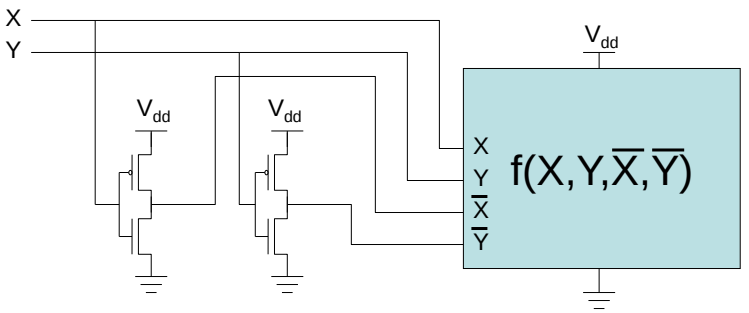
OTHER EXAMPLE: EXCLUSIVE-OR (XOR)

$f(X,Y) = \overline{X}.Y + X.\overline{Y}$

What to do about inverted variables?

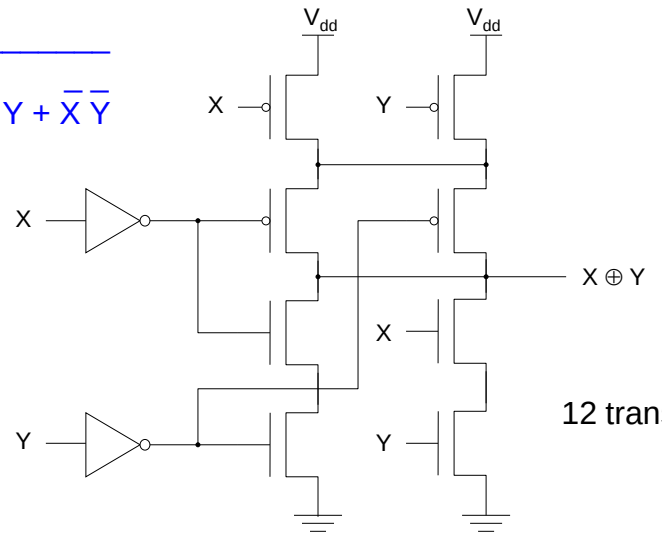
Make them inputs, too

$f(X,Y,\overline{X},\overline{Y}) = \overline{X}.Y + X.\overline{Y}$



EXAMPLE: EXCLUSIVE OR (XOR)

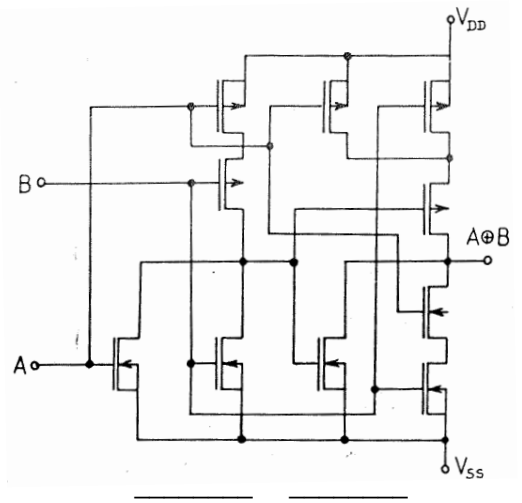
$X \oplus Y = X\,Y + \overline{X}\,\overline{Y}$



12 transistors

16

XOR (ANTIVALENCY) GATE



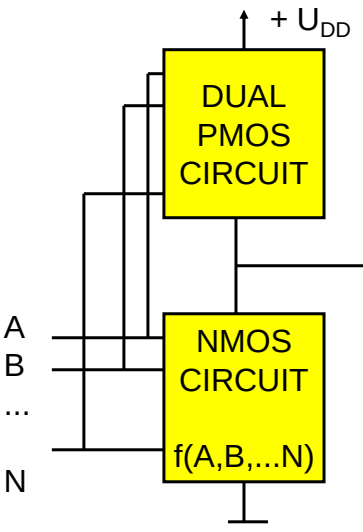
Series connection of two-input NAND gate and three-input complex gate

10 transistors

$$OUT = \overline{A + B} + A\,B = \bar{A}\,\bar{B} + A\,B = \bar{A}\,B + A\,\bar{B} = A \oplus B$$

17

CMOS COMPLEX GATES: GENERAL PRINCIPLE



The upper (load) network and the lower (control) network are duals of each other

CMOS COMPOUND GATE

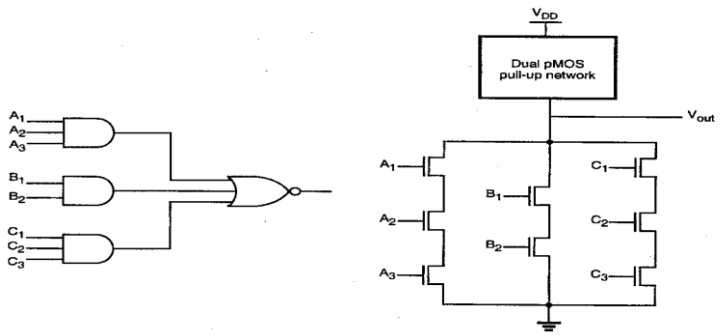
Design a circuit implementing $Y = (A + B + C)\,D$

Implement the negated function $\overline{Y} = \overline{(A + B + C)\,D}$

Add an inverter

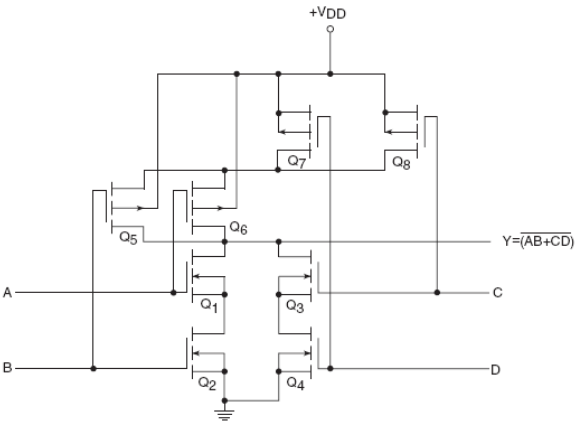
19

AOI (AND-OR-INVERT) CMOS GATE



AOI complex CMOS gate can be used to directly implement a sum-of-products Boolean function
The pull-down N-tree can be implemented as follows:
Product terms yield series-connected NMOS transistors
Sums are denoted by parallel-connected legs
The complete function must be an inverted representation
The pull-up P-tree is derived as the dual of the N-tree

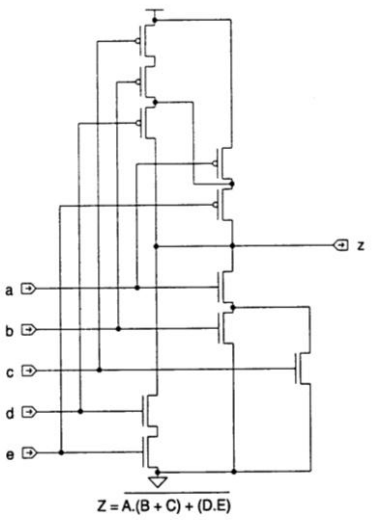
AND-OR-INVERT



Two-wide, two-input AND-OR-INVERT gate
(8 transistors)

21

CMOS COMPLEX GATE



Each logic function is duplicated for both pull-down and pull-up logic tree

- pull-down tree gives the zero entries of the truth table, i.e. implements the negative of the given function Z
- pull-up tree is the dual of the pull-down tree, i.e. implements the true logic with each input negative-going

Advantages: low power, high noise margins, design ease, functionality

Disadvantage: high input capacitance reduces the ultimate performance

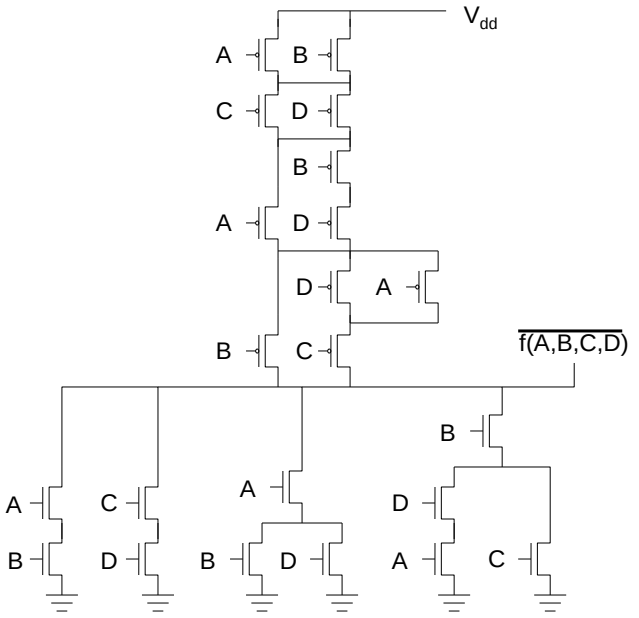
EXAMPLE OF A COMPLEX GATE

Complement
for PMOS=

(A+B)
. (C+D)
. (A+(B.D))
. (B+((D+A).C))

f(A,B,C,D) =

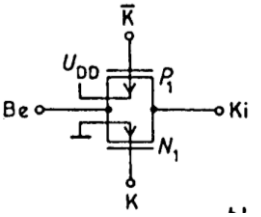
A.B
+ C.D
+ A.(B+D)
+ B.(D.A+C)



TRANSFER GATE

Transmission gates are the way to build “switches” in CMOS.

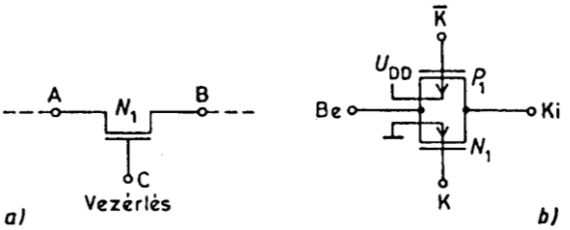
Both transistor types are needed:
nFET to pass zeros.
pFET to pass ones.



Architecture: nFET and pFET connected in parallel, gates driven in opposite phase.
The transmission gate is bi-directional (unlike logic gates and tri-state buffers).
Functionally it is similar to the tri-state buffer, but does not connect to V_{dd} and GND, so must be combined with logic gates or buffers.

Using transfer gates significant circuit simplifications can be realized.

MOS TRANSFER GATE



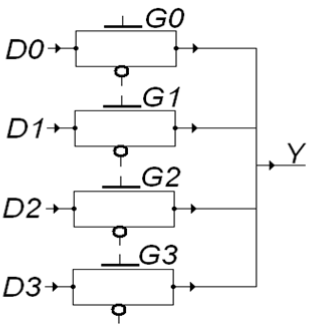
MOS transfer gates, a. n-MOS, b. CMOS implementation

n-channel: $U_{kiH}=U_H-U_T$, $U_{kiL}=U_L$; does not properly transfer HIGH
p-channel $U_{kiH}=U_H$, $U_{kiL}=U_L+U_T$; does not properly transfer LOW

Solution: CMOS – transfers both levels.

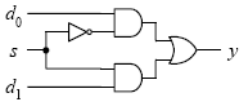
25

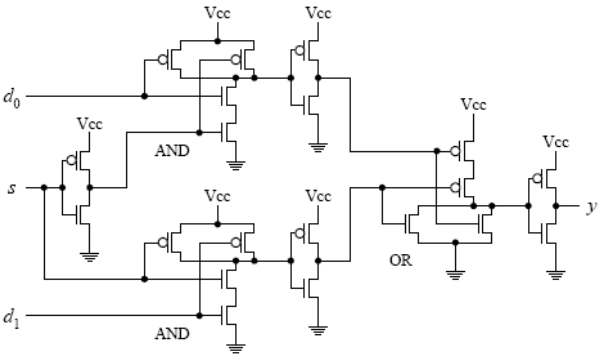
MULTIPLEXERS IN CMOS



4-to-1 multiplexer implemented with CMOS transfer gates.
Very transistor efficient solution!

MULTIPLEXER (1)

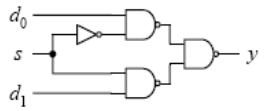


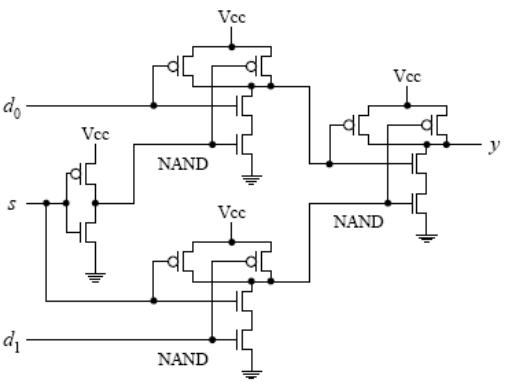


Using AND and OR gates

27

MULTIPLEXER (2)

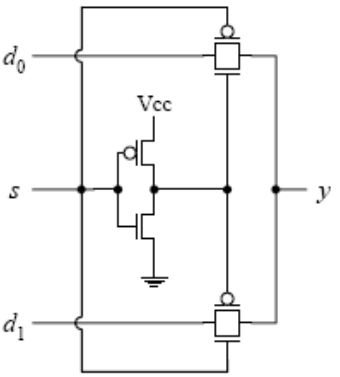




Using NAND gates

28

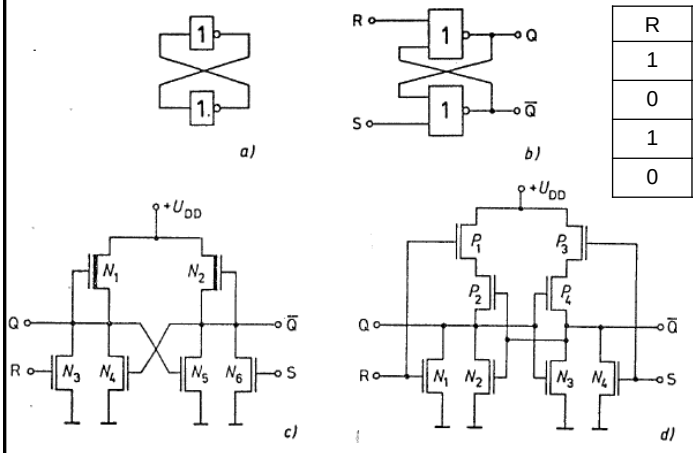
MULTIPLEXER (3)



Using transmission gates (6 transistors!)

29

RS FLIP-FLOP (LATCH)



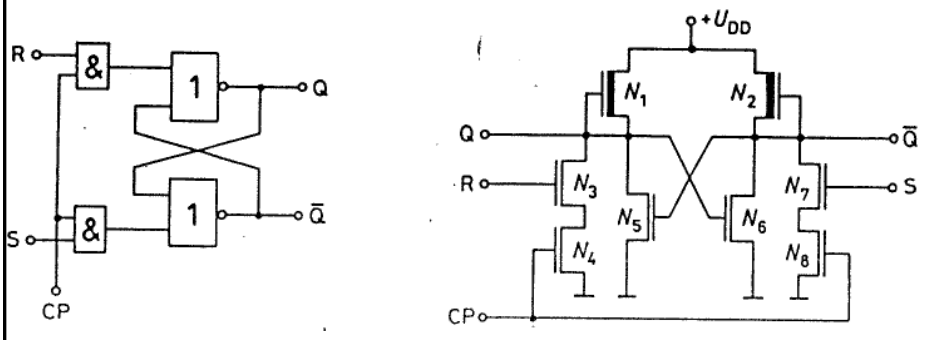
R	S	Q	Q(-)
1	1	0*	0*
0	1	1	0
1	0	0	1
0	0	Q**	Q(-)**

* forbidden state
** holding state

a) bistability principle, b) RS flip-flop (latch), c) depletion MOS load implementation, d) CMOS implementation

30

CLOCK CONTROLLED RS FLIP-FLOP

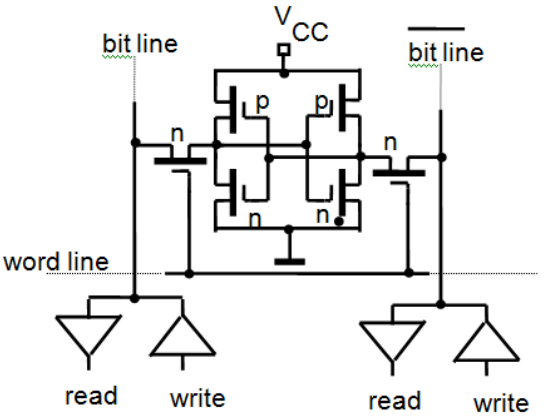


Logic diagram and NMOS implementation

Note the simplification achievesd by realizing the series connected AND and NAND gates with a complex gate.

31

CMOS STATIC RAM CELL

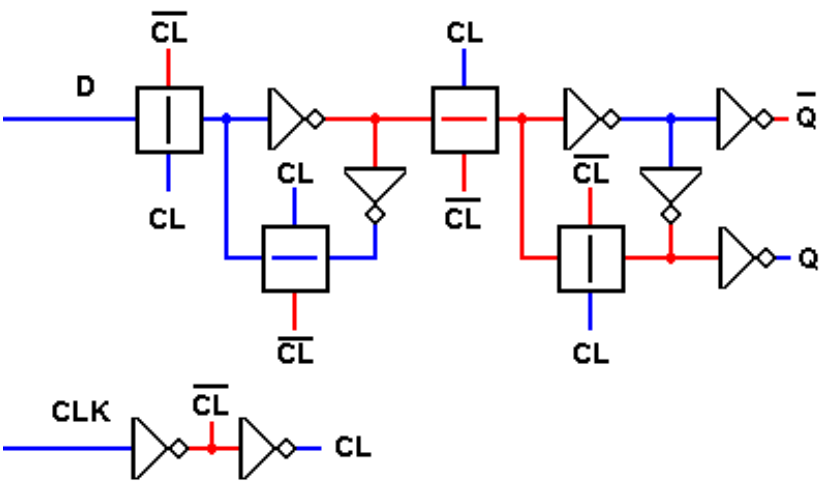


Six-transistor CMOS RAM memory cell: two cross-coupled CMOS inverters (RS flip-flop). R/W through two nMOS transistors

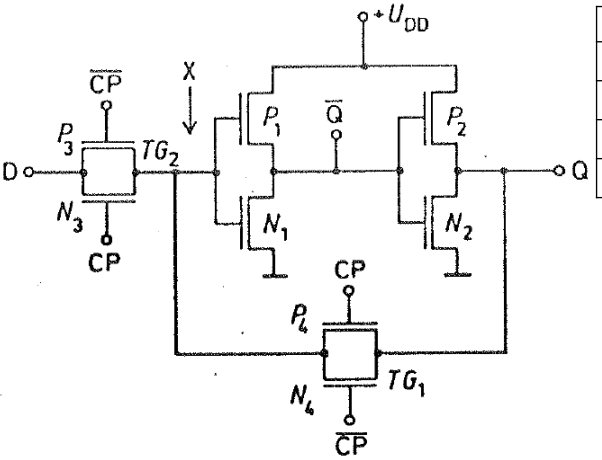
CMOS D FLIP-FLOP

- CMOS technology allows a very different approach to flip-flop design and construction. Instead of using logic gates to connect the clock signal to the master and slave sections of the flip-flop, a CMOS flip-flop uses *transmission gates* to control the data connections.

CMOS D FLIP-FLOP SCHEMATIC



D FLIP-FLOP (LATCH), CMOS

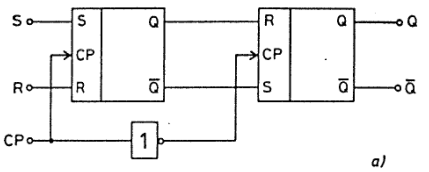


D	CP	Q	Q(-)
0	0	Q	Q(-)
0	1	0	1
1	0	Q	Q(-)
1	1	1	0

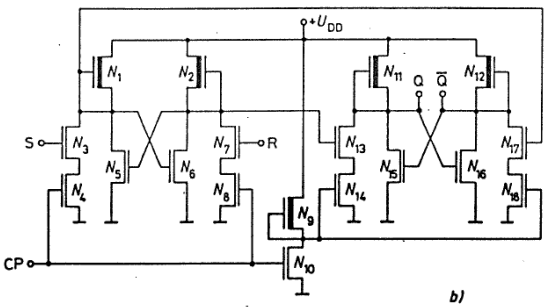
CP=1 ⇒ TG2 open, TG1 closed , no feedback, input level reaches output
CP=0 ⇒ TG2 closed, TG1 open, input separated, state holds (feedback!)
Requires only 8 transistors!

35

MASTER-SLAVE RS FLIP-FLOP



a)

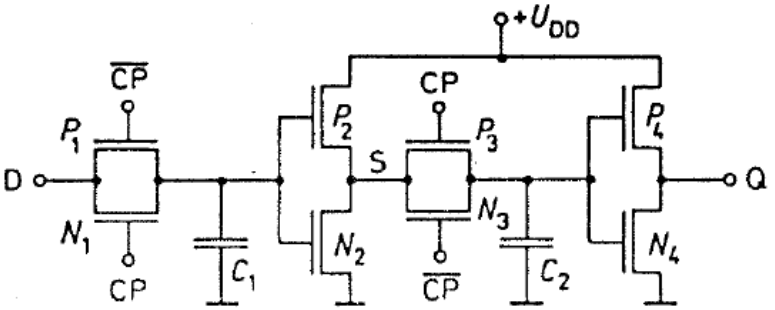


b)

Two RS flip-flops in series controlled by opposite phase clock
a) logic diagram, b) NMOS implementation

36

DYNAMIC MASTER-SLAVE D FLIP-FLOP



Signal levels are stored on capacitors C1 and C2, and is transferred by the clock signal:
CP=1, the input signal is transferred to C1 and to the output of INV1 (S)
CP = 0, input is separated, the signal is transferred to C2 and to the output.

Dynamic operation (refreshment is necessary), the capacitors are slowly discharged .

37

READ ONLY MEMORIES (ROM)

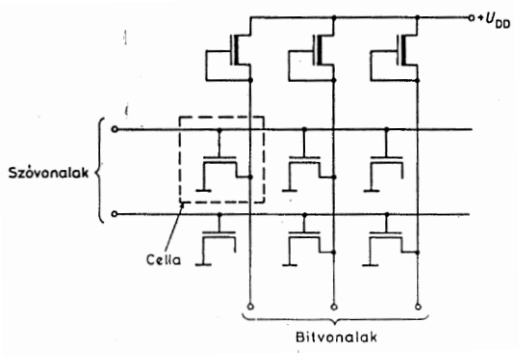
Recapitulation/review:

Read Only Memory (ROM)
Read Write Memory (RWM or RAM)

Programable ROM (PROM)
Erasable Programable ROM (EPROM) – UV light erasing
Electrically Erasable Programable ROM (EPROM) - memory transistors
Flash-EPROM

38

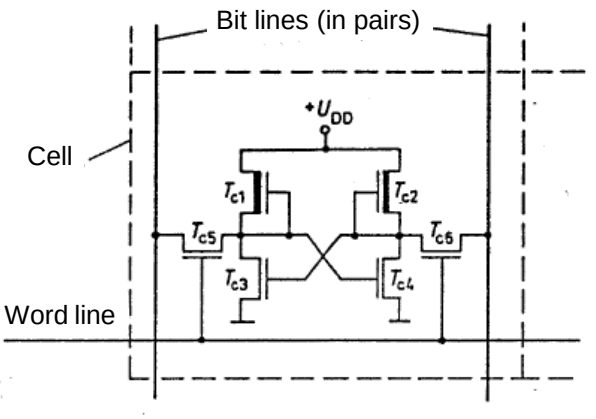
READ ONLY MEMORIES (ROM)



NMOS inverter type ROM functional circuit diagram. One bit – one driver.

39

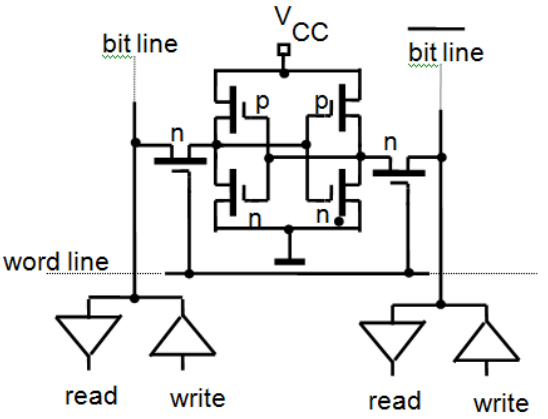
STATIC RAM (RWM)



Static NMOS RAM (RWM) cell. The storage element is the flip-flop (T1…T4 transistors) . The cell is connected to the bit lines by activating the world line. Reading and writing through the bit lines.

40

CMOS STATIC RAM CELL



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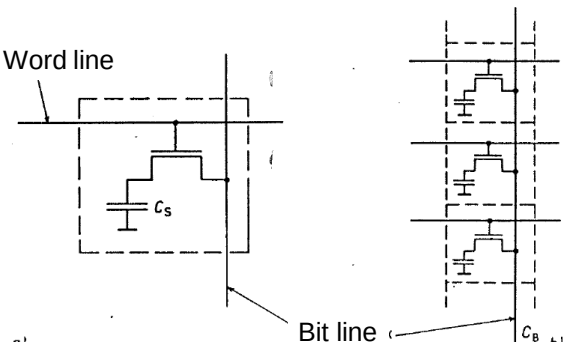
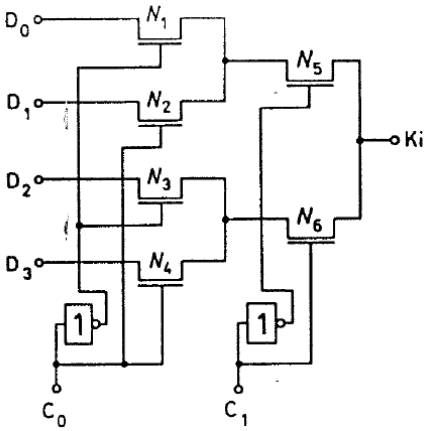
DYNAMIC RAM (RWM)



MOS dynamic RAM (RWM) cell. Activating the word lin opens the transistor, the capacitor is connected to the bit line.
The information is stored on the capacitor formed by the source and the earth line, the source area is appropriately increased. Periodic refreshment is necessary.

42

MULTIPLEXER

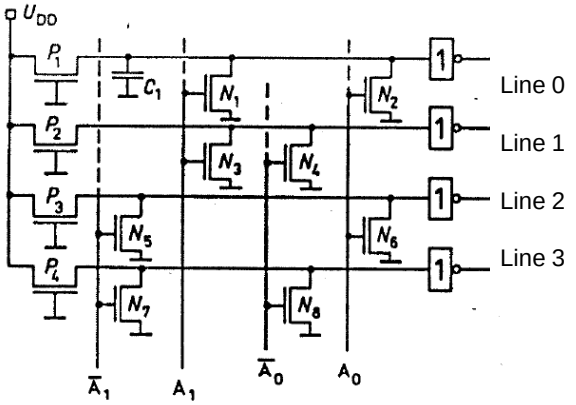


C0	C1	OUT
0	0	D0
0	1	D2
1	0	D1
1	1	D3

MOS multiplexer – circuit diagram and truth table.
It can be implemented using CMOS transfer gates, which yields a better defined HIGH level.

43

DECODER



A0	A1	OUT
0	0	LINE 0
0	1	LINE 2
1	0	LINE 1
1	1	LINE 3

Passive PMOS loaded NMOS decoder circuit diagram. A0A1 combination activates one of the output lines. Due to the output inverters, the output is active low.

44

FULL ADDER IMPLEMENTED IN CMOS

The simplest forms of the sum and carry function are (written in a form appropriate to CMOS implementation)

$$S = \overline{C}(A\,\overline{B} + \overline{A}\,B) + C(A\,B + \overline{A}\,\overline{B})$$

$$C_{out} = A\,B + C(A + B)$$

This is easily implemented using standard CMOS principles. The total transistor count is 34.

The disadvantage is that the circuit uses the negated values of the inputs too. Therefore the total transistor count is 34 + 6 = 40.

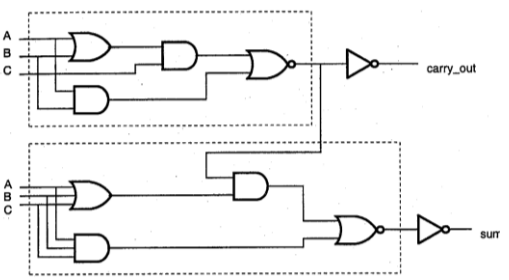
FULL ADDER IMPLEMENTED IN CMOS

This disadvantage can be avoided, if the negated value of the generated carry C_{out} is used to calculate the sum according to

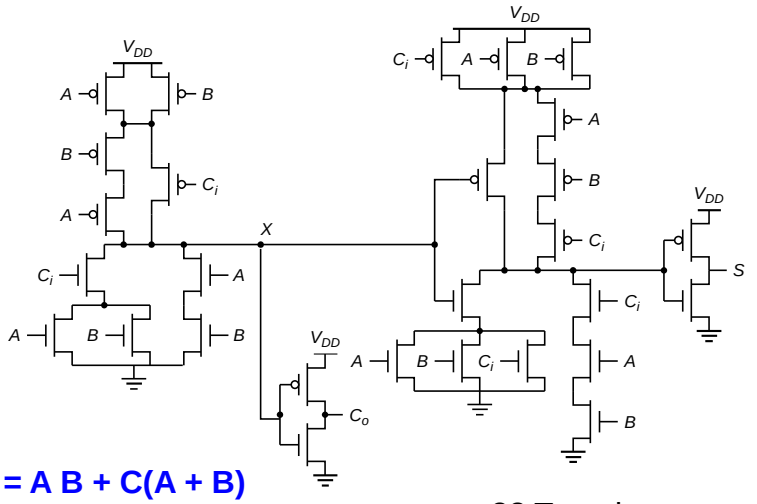
$$C_{out} = A\,B + C(A + B)$$

$$S = (A + B + C)\overline{C_{out}} + A\,B\,C$$

In this case the time delay of the sum will be larger, because three inverting operation is performed, but this is not relevant in a parallel (ripple-carry) adder, because the time necessary for a multi-bit addition is determined by the propagation time of the carry.



STATIC CMOS FULL ADDER



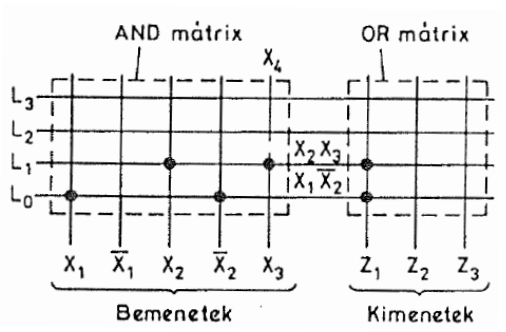
$C_{out} = A\,B + C(A + B)$

28 Transistors

$S = (A + B + C)\overline{C_{out}} + A\,B\,C$

PROGRAMABLE LOGIC DEVICES

Programmable logic array (PLA): general layout

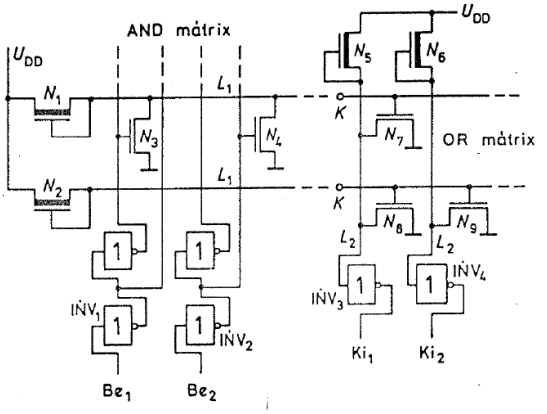


The realized function

$Z1 = X1\ \overline{X2} + X2\ X3$

48

PLD MOS IMPLEMENTATION



Based on De Morgan's theorem!
The *AND matrix* is a NOR circuit driven by the negated/inverted input variables, N3 and N4 are the drivers, N1 and N2 are the loads.
The *OR matrix* is also a NOR circuit the output inverters establish the high levels. N7, N8, and N9 are the parallel drives, N5 and N6 are the loads.

TRANSISTOR COUNT

The *transistor count* is the number of transistors on an integrated circuit (IC). Transistor count is the most common measure of IC complexity, although there are caveats. For instance, the majority of transistors are contained in the cache memories in modern microprocessors, which consist mostly of the same memory cell circuits replicated many times. The rate at which transistor counts have increased generally follows *Moore's law*, which observed that the transistor count doubles approximately every two years. As of 2016, the largest transistor count in a commercially available single-chip processor is over 7.2 billion the Intel *Broadwell-EP XEON*. In other types of ICs, such as field prograímmable gate arrays (FPGAs), Intel's (previously Altera) Stratix 10 has the largest transistor count, containing over 30 billion transistors.

TRANSISTOR COUNT

Transistor count for generic logic functions is based on static CMOS implementation.

Function	transistor count	Function	transistor count
NOT/INV	2	1-bit adder full	28
BUFFER	4	1-bit adder/subtractor	48
NAND, NOR 2-input	4	D flip-flop gated	8
AND, OR 2-input	6	D FF edge triggered w. reset	12
NAND, NOR 3-input	6		
XOR	6	8-bit multiplier	3,000
XNOR	8	16-bit multiplier	9,000
MUX 2-input with TG	6	32-bit multiplier	21,000
MUX 4-input with TG	18		
MUX 4-input	24		

51

REVIEW QUESTIONS

1. Describe the difference between the bipolar integrated circuits and MOS integrated circuits.

2. Describe the characteristics of MOS logic.

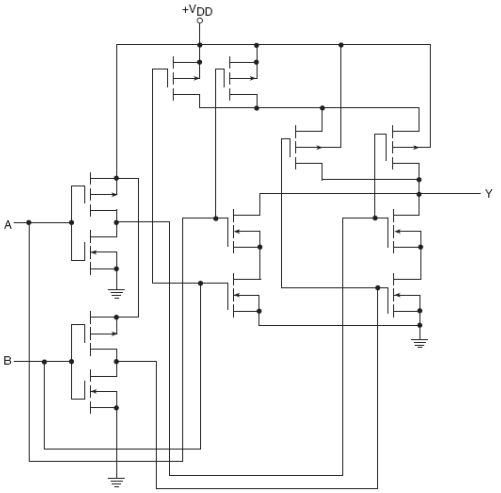
3. With the help of relevant circuit schematics, briefly describe the operation of CMOS NAND and NOR gates.

4. Draw a 4-input CMOS NAND gate. Repeat for a 4-input NOR gate with CMOS.

52

PROBLEMS AND EXERCISES

1. Write the logic expression for the CMOS circuit below.



53

PROBLEMS AND EXERCISES

2. a. Draw the NMOS or CMOS transistor level circuit of the complex gate **F = (A + B) C**.
2. b. Draw the NMOS or CMOS transistor level circuit of the complex gate **F = A B + C**.

3. Show that the sum (**S**) function of the one-bit full adder can be expressed in terms of the three inputs (**A**, **B**, and $\mathbf{C_{in}}$) and of the carry out ($\mathbf{C_{out}}$) as

$$\mathbf{S = (A + B + C_{in})\overline{C_{out}} + A\,B\,C_{in}}$$

54

PROBLEMS AND EXERCISES

4. Draw the circuit diagram of a 2-to-1 multiplexer based on CMOS transfer gates.

5. Draw the circuit diagram of a nMOS memory cell and of a CMOS memory cell.

END