DIGITAL TECHNICS

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Óbuda University,
Microelectronics and Technology Institute

10. LECTURE (LOGIC CIRCUITS, PART 3)
TTL, SCHOTTKY TTL, BiCMOS, ECL

1st (Autumn) term 2018/2019

10. LECTURE

1. Logic circuit families, introduction and historical development
2. ”Classical” and high performance („advanced”) logic families, performance comparisons
3. Advanced Schottky TTL logic families
4. Advanced CMOS circuits and logic families
5. BiCMOS logic families

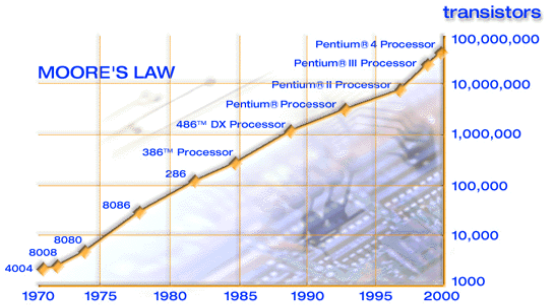
MOORE'S LAW

Gordon Moore (co-founder of Intel) predicted in 1965, just four years after the first planar integrated circuit was discovered, that the number of transistors per integrated circuit would double every 18 months.

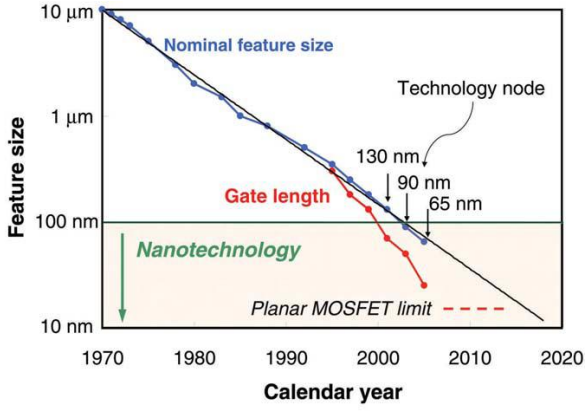
He forecast that this trend would continue through 1975.

Moore's Law has been maintained for far longer, it has become a universal law of the entire semi-conductor industry. It still holds true as we enter the second decade of new century.

Moore's law is about human ingenuity not physics.



MOORE'S LAW



The INTEL's gurus: **A. Groove, R. Noyce G. Moore INTEL,1970**

Logic technology node and transistor gate length versus calendar year. Note:

mainstream Si technology is nanotechnology.

THE HUNGARIAN CONNECTION

Andy Grove (1936-2015) alias Gróf András

EETimes 3/2016:
Andy Grove a Hungarian immigrant who survived Nazi occupation (and the arrow-cross Hungarian Nazi terror…) and vent on to be instrumental in the formation of Intel Corp. And its rise to become the biggest semiconductor company in the world, died Monday (March 21) at he age of 79.

Though not credited as a co-founder, Grove was present for Intel1s early history, beginning in 1968.

Company's president 1979 to 1997,
CEO from 1987 to 1998,
Chairman of board of directors from 1997 to 2005.

Grove was an enormously influential figure in the semiconductor industry and beyond. At Intel, he presided over the company's transformation from a supplier of memory chips into the world's biggest microprocessor vendor.

THE HUNGARIAN CONNECTION

During Grove's tenure as CEO Intel's market capitalization increased from $4billion to $197billion. During that time Intel's annual revenue increased from $1,9 billion to more than $26 billion (about 7000 billion HUF, roughly 25 % of Hungary's GDP).

Grove immigrated to the U.S. in 1957 after surviving both the Nazi occupation and arrow-cross terror and the subsequent repressions in and Sovietization of Hungary. He studied chemical engineering at the City College of New York and completed his Ph.D. at the University of California-Berkeley in 1993.

Grove was hired to Fairchild Semiconductor by Gordon Moore as a researcher in 1963. When Moore and Robert Noyce left Fairchild to found Intel in 1968, Grove was their first hire.

THE HUNGARIAN CONNECTION

„Andy approached corporate strategy and leadership in ways that continue to influence prominent thinkers and companies around the world", said Intel Chairman Andy Bryant. „ *He combined the analytic approach of a scientist with an ability to engage others in a honest and deep conversation, which sustained Intel's success over a period that saw the rise of the personal computer, the Internet and Silicon Valley*."

LOGIC CIRCUITS GENERATIONS AND FAMILIES

The circuit technologies are the relevant factors which determine and characterize the generations of logic circuits.

A logic family of monolithic digital integrated devices is a group of electronic logic gates, flip-flops, etc., constructed using one of several different designs and technology, usually with compatible logic levels and power supply characteristic within the family.

Before the widespread use of integrated circuits, various vacuum-tube and solid-state logic systems were in use, but these were never as standardized and interoperable as the IC devices.

LOGIC CIRCUIT GENERATIONS

1930s, relay circuits, Bell Labs
(driving force: telephone exchange switching)

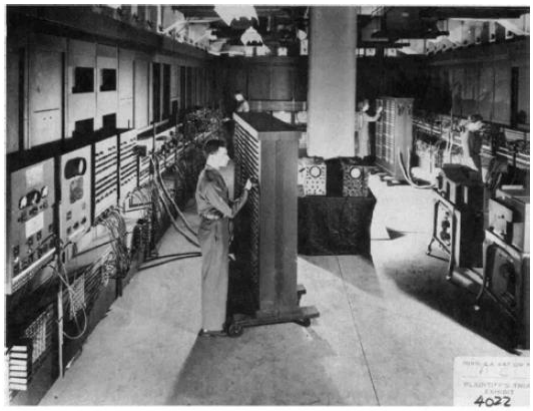
1940s, vacuum tubes e.g. ENIAC, built in 1946 (electronic numerical integrator and calculator), calculated the trajectory of an artillery shell in only 30 sec. Large and expensive…

18 thousand vacuum tubes
60 thousand pounds (27 thousand kg)
16200 cubic feet (480 m^3)
174 kW

(c.f. four-operation hand-held calculator appr. 9 000 transistors)

(driving force: military applications, artillery shell trajectory calculations)

ENIAC: 1946



Further comment: Failure rate of a commercial vacuum tube is about 1/2000 per hour, of an industrial or high-reliability type is about 10 times smaller.
Estimated failure rate of the ENIAC **about one per hour (!)**

LOGIC CIRCUIT GENERATIONS: ENIAC

ENIAC could add 5000 numbers in one second.

The amount of energy ENIAC expended to compute a single shell trajectory was comparable to that of the explosive discharge required to actually fire the shell.

ENIAC was still the fastest computer on the Earth nine years later, when it was turned off because the US Army could no longer justify the expense of operating and maintaining it.

LOGIC CIRCUIT GENERATIONS (2)

1950/1960 semiconductor diode and transistor circuits

- RTL resistor-transistor-logic
- DTL diode-transistor-logic
- ECL emitter-coupled logic (later)

From 1961 SSI (above listed on one chip)

1960s TTL (transistor-transistor logic), Sylvania, then Texas Instruments, the TI system later became the *de-facto* industry standard

After 1960/1970: MOS metal oxide semiconductor: pMOS (1960s) then nMOS (1970s)

1980s CMOS (complementary metal-oxide-semiconductor) introduced in 1968 by RCA

LOGIC CIRCUIT FAMILIES: FEATURES

The feature to be concerned of IC logic families:

- Fan-out
  - The no. of standard loads can be connected to the output of the gate without degrading its normal operation
  - Sometimes the term *loading* is used
- Power dissipation
  - The power needed by the gate
  - Expressed in mW
- Propagation delay
  - The average *transition-delay time* for the signal to propagate from input to output when the binary signal changes in value
- Noise margin
  - The unwanted signals are referred to as *noise*
  - Noise margin is the *maximum noise* added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output

TRANSISTOR-TRANSISTOR LOGIC

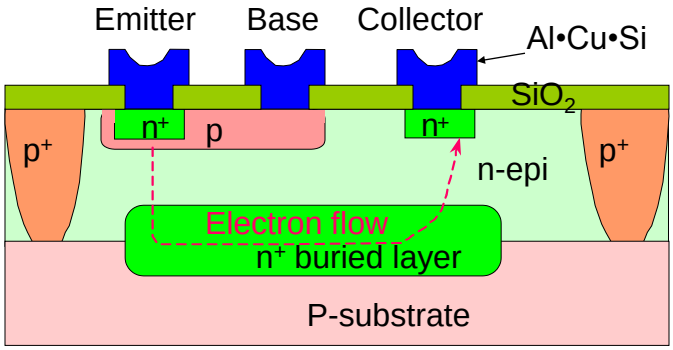
Mostly widely used IC technologies.

First circuit family: Texas Instruments
Semiconductor Network

74 Series (standard)& 54 Series (military specification)
Combination of BJTs, diodes, and resistors.
Implement logic function, e.g., NAND, NOR, etc.
Package (DIP, SMT)

The TTL system is based on the silicon bipolar transistor technology. It is a so called „saturation" logic system, because the transistors are driven to saturation or near-saturation

Si NPN (PLANAR) TRANSISTOR



The workhorse of the bipolar ICs is the Si npn transistor

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THE (BIPOLAR) TRANSISTOR

Probably no single development of modern physical science has touched so many people's lives so directly as has world-shaking invention of the transistor.
Xmas 1947: Bell scientists realized the world's first successful solid-state amplifier.
The transistor revolutionized electronic communication devices, as well as making practical the extensive development of high-speed, high-capacity computers. In regard to the latter, an important feature of the transistor is the low amount of energy required per bit of information processed and its extremely long operational life.
Its invention was truly a landmark, and it is small wonder that a Nobel prize of physics was awarded in 1956 to the men primarily responsible: John Bardeen, Walter Brattain, and William Shockley.

TRANSISTOR STORY: MILESTONES

- 1925-1928 J. E. Lilienfeld, field effect transistor patents
- 1947 J. Bardeen, W. H. Brattain (Bell Labs), point contact transistor (physics Nobel prize1956)
- 1948 W. Shockley (Bell Labs), pn junction, bipolar transistor (physics Nobel prize, 1956)
- 1958-1959 J. Kilby (Texas Instruments) integrated circuit (physics Nobel prize, 2000)
- 1958-1961 R. Noyce (Fairchild) integrated circuit (he did not live long enough for the Nobel prize…)

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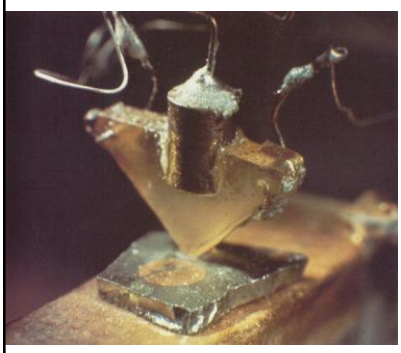
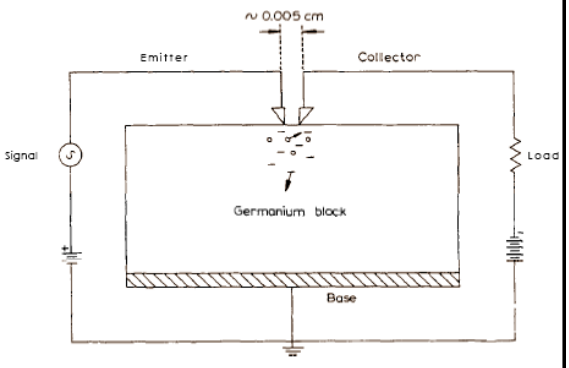
THE POINT CONTACT TRANSISTOR: THE FIRST SEMICONDUCTOR AMPLIFIER





William Bradford SHOCKLEY, John BARDEEN, Walter Houser BRATTAIN, physics Nobel prize in1956

TRANSISTOR TRANSfer resISTOR

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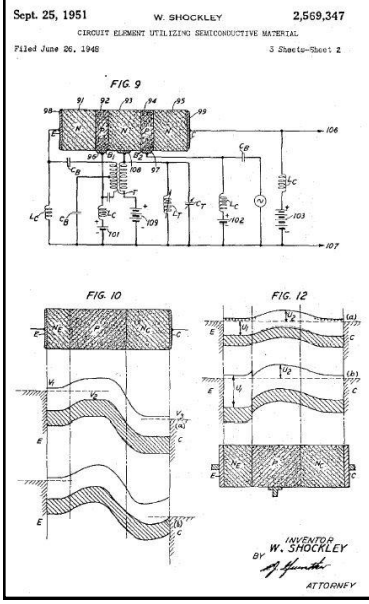
THE BIPOLAR TRANSISTOR PATENT


Sept. 25, 1951 W. SHOCKLEY 2,569,347

CIRCUIT ELEMENT UTILIZING SEMICONDUCTIVE MATERIAL

Filed June 26, 1948 3 Sheets-Sheet 2

FIG. 9

FIG. 10

FIG. 12

INVENTOR W. SHOCKLEY

BY

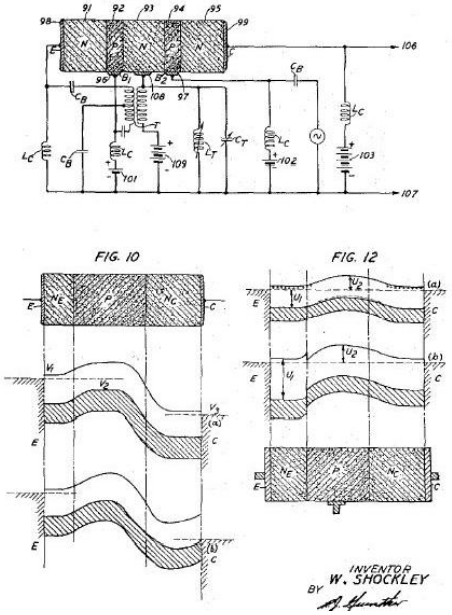
ATTORNEY

A page from the original patent by W. Shockley:

CIRCUIT ELEMENT UTILIZING SEMICONDUCTOR MATERIAL

Filed: June 26, 1948
Published: Sep 25, 1951, 2569347

THE BIPOLAR TRANSISTOR PATENT



1947 (48) - The first point-contact germanium transistor

William Bradford Shockley (1910-1989)

John Bardeen (1908-1991)

Walter Houser Brattain (1902-1987)

The Nobel Prize in Physics 1956:
"for their researches on semiconductors and their discovery of the transistor effect"

THE PEOPLE

John Bardeen (1908-1987)

A brilliant theorist, *Bardeen* brought his keen understanding to the transistor team by explaining effects found in early transistor experiments.

Bardeen won the Nobel prize in 1956 as co-inventor of the transistor, and again in 1972 as co-developer of the theory of superconductivity at low temperatures.

Bardeen left Bell Labs in 1951 to join the faculty at University of Illinois, where he dedicated himself to research superconductivity.

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THE PEOPLE

Walter H. Brattain (1902-1987)
An ingenious experimenter, *Brattain*'s creativity and persistence enabled the team to triumph over difficult technical obstacles to demonstrate the transistor effect**.**

One of the applications of the transistor that *Brattain* was most proud of was the development of the transistor radio. "*This has made it possible for even the most underprivileged people to listen. Nomads in Asia, Indians in the Andes, and natives in Haiti have these radios, and at night they can gather together and listen.*" He added, "*All peoples can now, within limits, listen to what they wish, independent of what dictatorial leaders might want them to hear*." He did admit he wasn't particularly pleased to listen to very loud rock and roll.

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World's first pocket radio (mid 50'ies)

Price $ 49.95

To compare:

In 1964 you could be a tourist in Western Europe for 5 $/day

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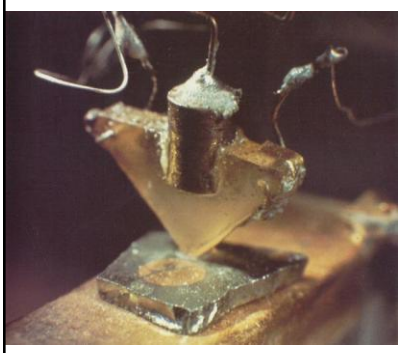
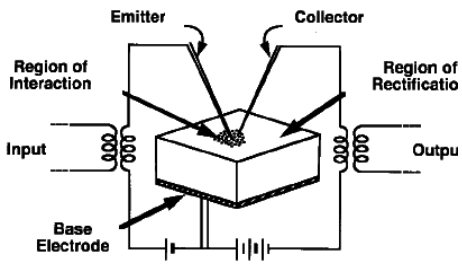
THE PEOPLE

William Shockley (1910-1989)
The brilliant director of the transistor effort, *Shockley*'s research in the behavior of electronics in crystals introduced him to Bardeen and Brattain, who aided him in his experimentation to build working models of transistor mechanisms. Spurned on by their demonstration of a working point-contact transistor, *Shockley* created the junction transistor, which became the fundamental structure of transistor developments to come.
Shockley left Bell Labs in 1955 to establish Shockley Semiconductor Laboratory (part of Beckman Instruments, Inc.), an effort that was instrumental in the birth of Silicon Valley and the electronics industry. Several of his former employees left his company to found what later became Intel, the most successful microprocessor company in the world. 25

THE POINT CONTACT TRANSISTOR: THE FIRST SEMICONDUCTOR AMPLIFIER





Schematic diagram of the first transistor

William Bradford SHOCKLEY, John BARDEEN, Walter Houser BRATTAIN, physics Nobel prize in1956

TRANSISTOR TRANSfer resISTOR

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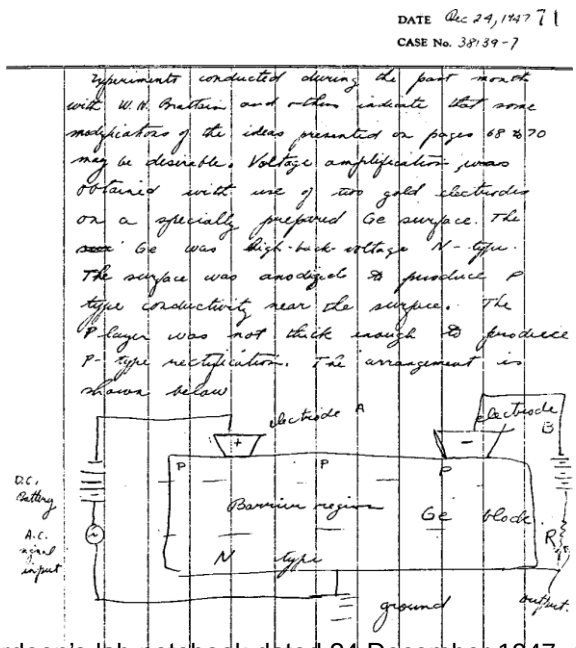
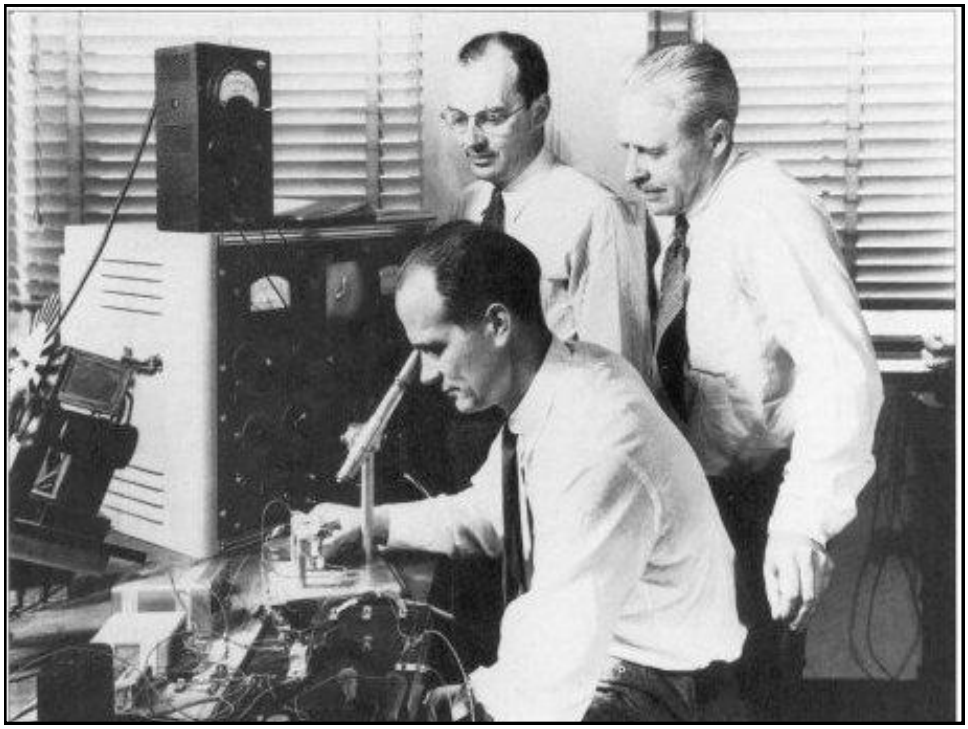
NAMING THE INVENTION

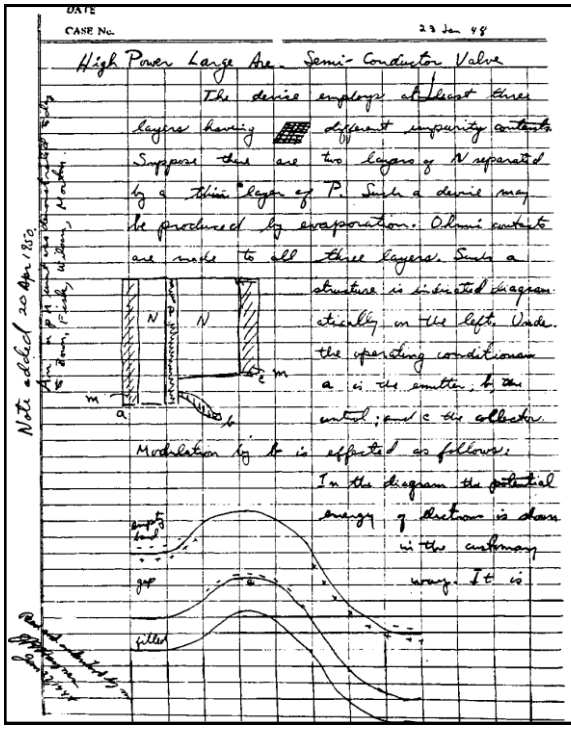
Naming The Invention

- **Pierce suggested *transistor* since electric field modulating resistance transverse to minority-carrier current**
- **Pierce apparently also noted point-contact transistor dual of vacuum tube from circuit point of view**
  - Therefore, electrical dual of transconductance, important parameter of vacuum tube, was transresistance, shortened to ***transistor***
- **Another interpretation noted prefix "trans" designates translational property of device, while root "istor" classified it as solid circuit element as with resistor, varistor and thermistor**



Entry in Bardeen's lab notebook dated 24 December 1947, giving his conception of how the point-contact transistor functions.





DATE 23 Jan 48
CASE No.

High Power Large Area Semi Conductor Valve

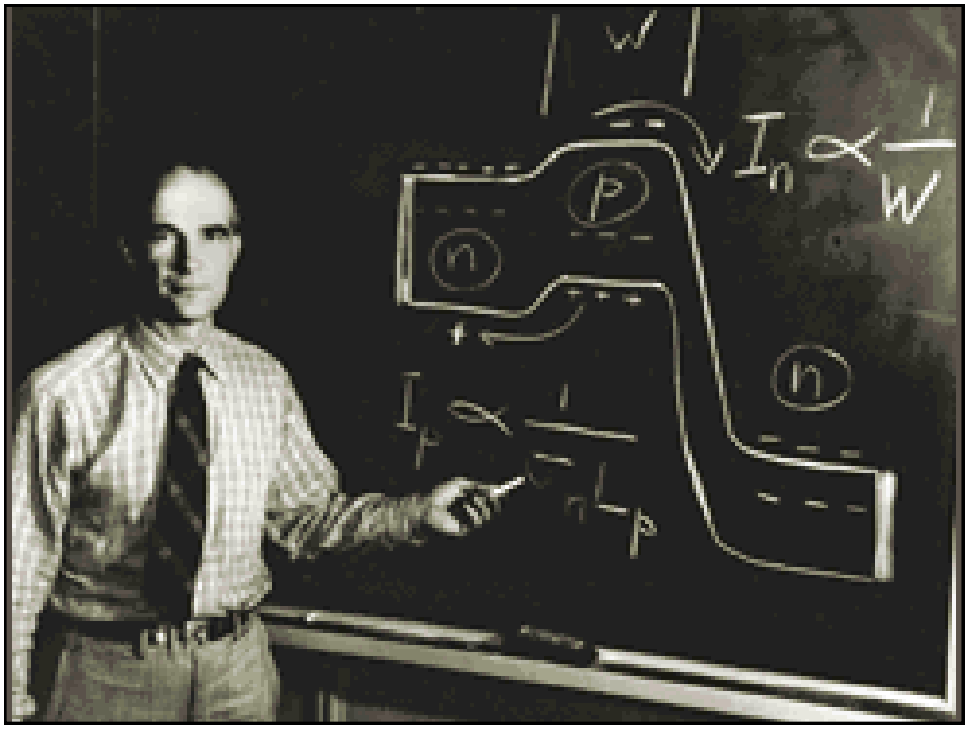
The device employs at least three layers having different impurity contents. Suppose that are two layers of N separated by a thin layer of P. Such a device may be produced by evaporation. Ohmic contacts are made to all three layers. Such a structure is indicated diagramatically on the left. Under the operating conditions a is the emitter, b the control; and c the collector.

Modulation by b is effected as follows:

In the diagram the potential energy of electrons is drawn in the customary way. It is

Noted & dated 20 Apr. 1953

Entry in Shockley's lab notebook dated 23 January 1948 recording his conception of the junction transistor. He wrote this page at home on a piece of paper, which he later pasted into his notebook.



THE MOSES OF SILICON VALLEY

SENIOR STAFF of the Shockley Semiconductor Laboratory toast their boss at a luncheon the day after the announcement of his Nobel Prize in 1956. These are the men who introduced Bell Laboratories' silicon technology to California. Gordon Moore is sitting at the far left; Robert Noyce is standing fourth from left and Jay Last is standing at the far right, just to the right of William Shockley, who is seated at the end of the table. (Courtesy of Intel Corporation.)

1960: THE Si IC PATENT (FAIRCHILD)

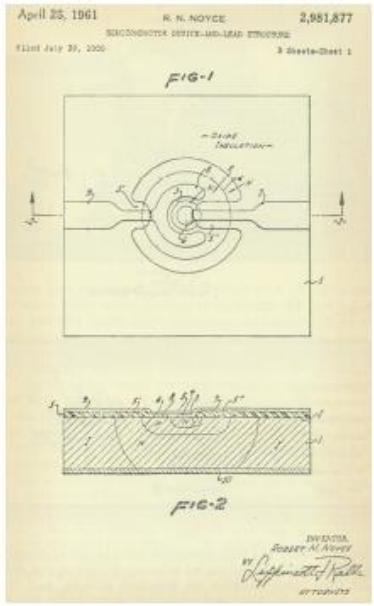

April 25, 1961 R. N. NOYCE 2,981,877

FIG-1

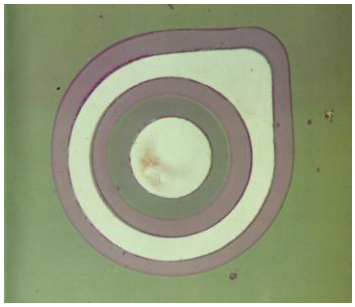
FIG-2

A page from the original patent by R. Noyce:

SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE

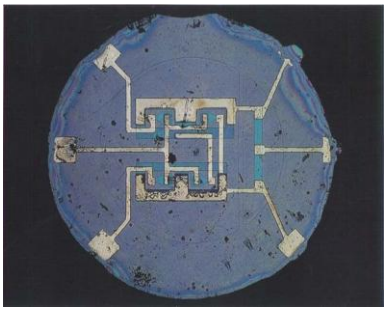
Filed: July 2?, 1960
Published: April 25, 1961, 2981877

Si INTEGRATED CIRCUIT

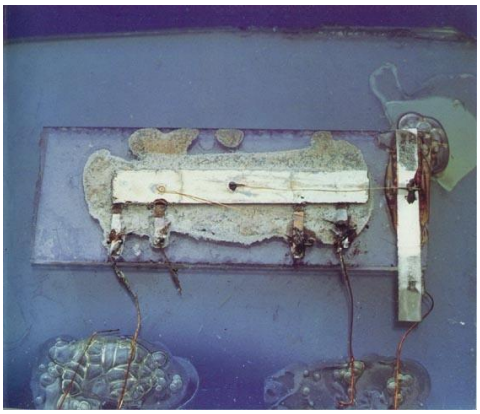


1959: planar process
Jean Hoerni and Robert Noyce

1961: first commercial planar IC
(two transistors in a flip-flop circuit)
Fairchild

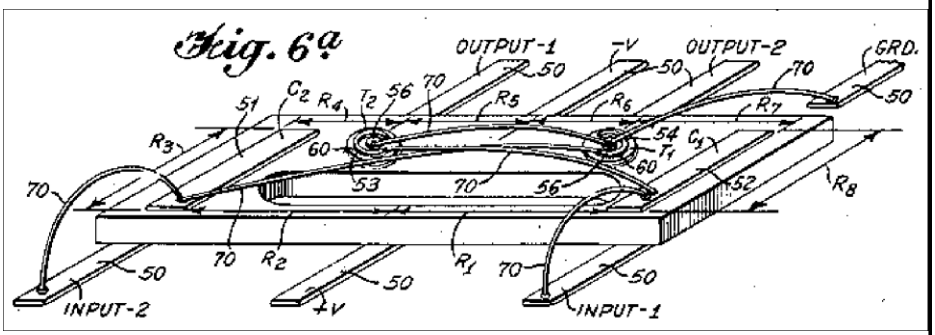


1958: INTEGRATED CIRCUIT

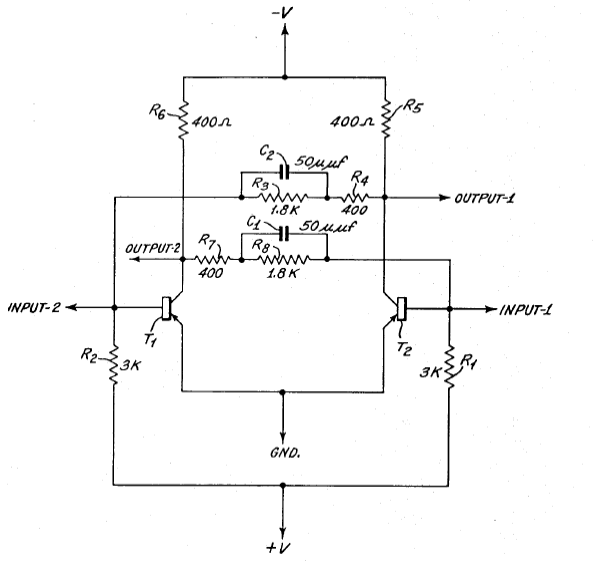


1958: first integrated circuit (Ge) *Jack Kilby*, Texas Instruments Physics Nobel Prize 2000 (shared with *Zhores I. Alferov* and *H. Kroemer*)

KILBY'S PATENT



Germanium flip-flop using mesa transistors, bulk resistors, diffused capacitors, and air isolation of the components. From US Patent 3,138,743.



June 23, 1964 J. S. KILBY 3,138,743

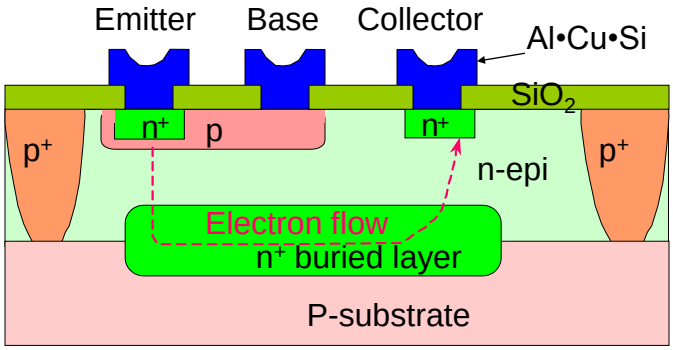
MINIATURIZED ELECTRONIC CIRCUITS

Filed Feb. 6, 1959 4 Sheets-Sheet 1

IC: Si BIPOLAR TECHNOLOGY

- Technology optimization: to optimize the Si npn transistor.
- Components: bipolar transistor, diode, resistor, capacitor.
- Transistor (and all other components) in-plane structure – planar technology.

Si NPN (PLANAR) TRANSISTOR



The workhorse of the bipolar ICs is the Si npn transistor

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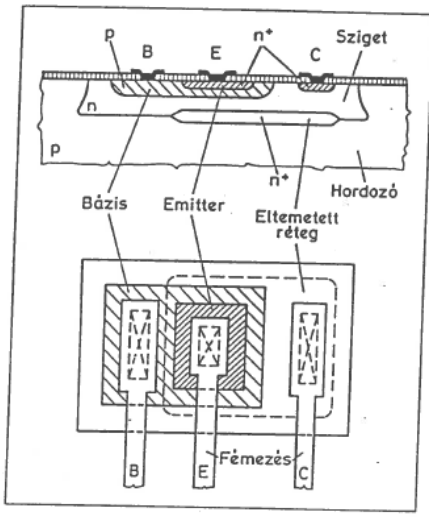
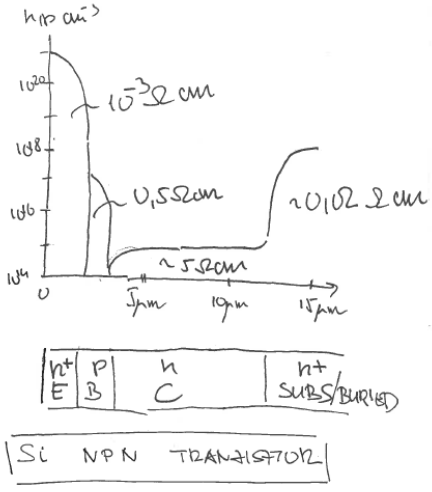
Si NPN (PLANAR) TRANSISTOR





IC: THE Si BIPOLAR TRANSISTOR

Typical Si npn transistor parameters

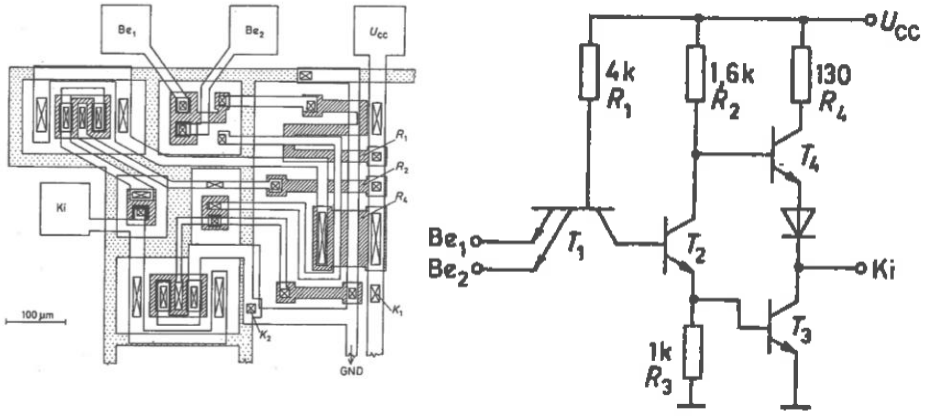
Region	V_{BE} (V)	V_{CE} (V)	Current Relation
Cutoff	< 0.6	Open circuit	$I_B=I_C=0$
Active	0.6-0.7	> 0.8	$I_C = h_{FE}I_B$
Saturation	0.7-0.8	0.2	$I_B \geq I_C/h_{FE}$

IC: THE Si BIPOLAR TRANSISTOR

- Typical dimensions:
  - emitter diffusion ~(2-2.5) μm
  - base diffusion ~4 μm
  - n-epitaxial layer (collector) ~10 μm
  - emitter window (small current transistor, ~1 mA)
    - (10-15) x (10-15) μm

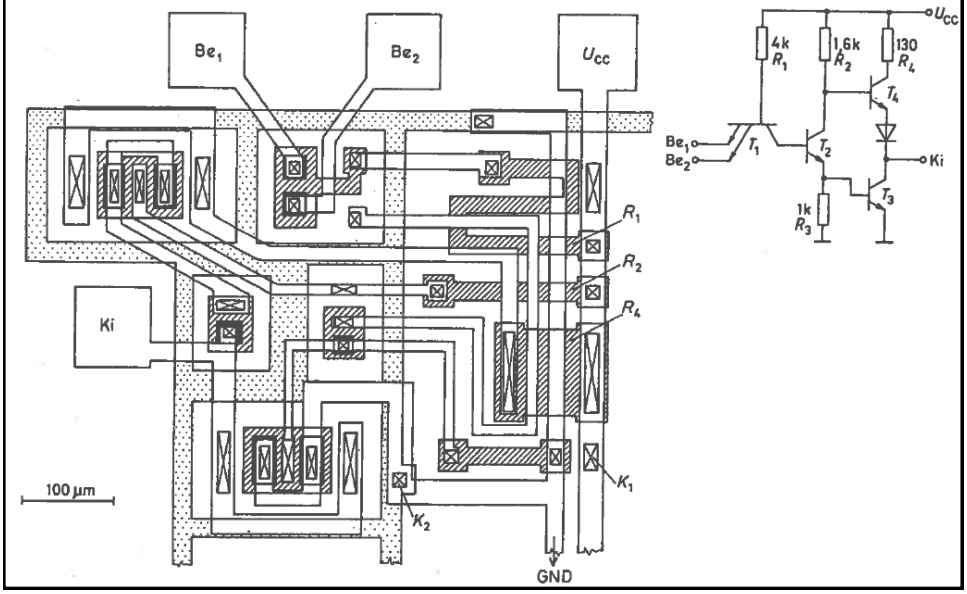
E.g. in a TTL circuit one emitter is 16 x 16 μm, the nominal input current is max 1.6 mA (current density 6.25 A/mm^2).

STANDARD TTL NAND GATE



Standard 2-input TTL NAND gate circuit.
Layout of dual 4-input NAND gate circuit.
Size: emitter window of the input multiemitter transistor:
16x16 µmsq

STANDARD TTL NAND GATE



RECALL: CONCEPTUAL STRUCTURE OF LOGIC GATES

Input lines

Output lines

Generic circuit layout of digital gates

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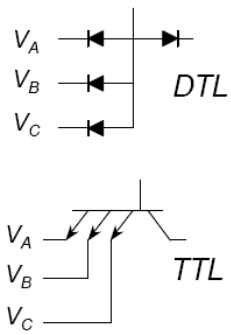
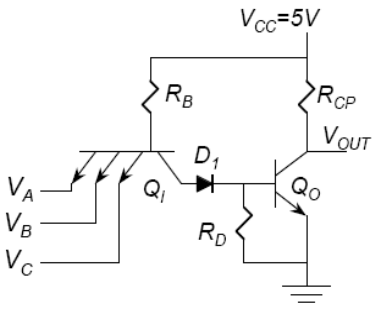
FROM DTL TO TTL ARCHITECTURE





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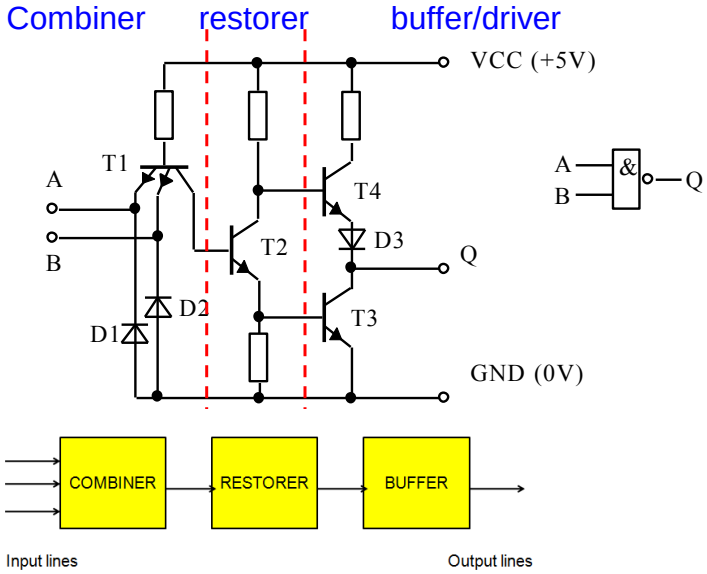
(BASIC/STANDARD) TTL GATE (NAND)



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TRANSISTOR-TRANSISTOR LOGIC TTL

The original basic TTL gate was a slight improvement over the DTL gate.

There are several TTL subfamilies or series of the TTL technology.

Has a number start with 74 and follows with a suffix that identifies the series type, e.g. 7404, 74S86, 74ALS161.

Three different types of output configurations:

1. open-collector output
2. Totem-pole output
3. Three-state (or tristate) output

74 – standard

54 – military

84 – industrial (discontinued)

TTL SERIES

• STANDARD		OBSOLOTE!
• SCHOTTKY	S	IN DECLINE/OBSOLOTE
• LOW-POWER SCHOTTKY	LS	IN DECLINE/OBSOLOTE
• ADVACED SCHOTTKY	AS	IN DECLINE
• FAST ADVANCED SCHOTTKY	F	
• ADVACED LOW-POWER SCHOTTKY	ALS	

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SCHOTTKY TTL: AN INTRODUCTION

Transistor in bipolar logic (standard TTL) are saturated switches - minority carrier storage limits the speed of the device.

Variations of the standard TTL design to reduce these effects and improve speed, power consumption, or both.

”Schottky transistors” i.e. junction transistors with integrated Schottky barrier clamping diodes between the collector and basis reduce or prevent charge storage, leading to faster switching gates.

Incorporating Schottky barrier diodes into the TTL design, the switching speed can be reduced to 2 ... 5 nsec, a half or full order of magnitude improvement with respect to conventional design.

SCHOTTKY DIODE I-V CHARACTERISTICS

- Schottky diode is a metal-semiconductor (MS) diode
- Historically, Schottky diodes are the oldest diodes
- MS diode electrostatics and the general shape of the MS diode I-V characteristics are similar to p^+n diodes, but the details of current flow are different.
- Dominant currents in a p^+n diode

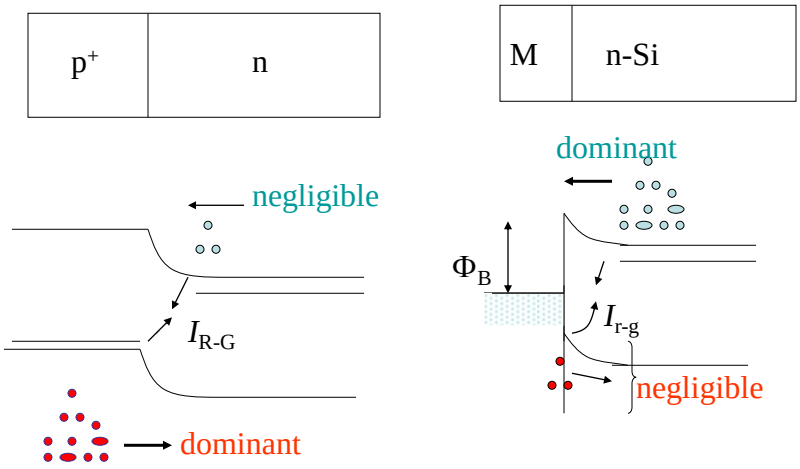
– arise from recombination in the depletion layer under small forward bias.

– arise from hole injection from p^+ side under larger forward bias.

- Dominant currents in a MS Schottky diodes

– Electron injection from the semiconductor to the metal.

CURRENT COMPONENTS IN p^+n and MS SCHOTTKY DIODES



I-V CHARACTERISTICS

$$I = I_S\left(e^{\frac{qV_A}{kT}} - 1\right) \quad \text{where} \quad I_S = A\mathcal{A}^* T^2 e^{-\frac{\Phi_B}{kT}}$$

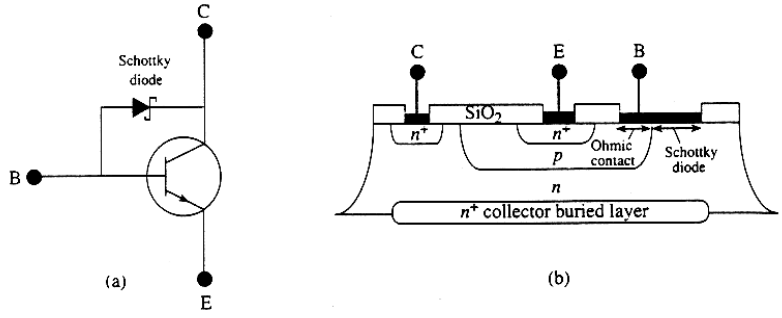
where Φ_B is Schottky barrier height, V_A is applied voltage, A is area, and A^* is Richardson's constant.

The reverse leakage current for a Schottky diode is generally much larger than that for a p^+n diode.

Since MS Schottky diode is a majority carrier devices, the frequency response of the device is much higher than that of equivalent p^+ n diode.

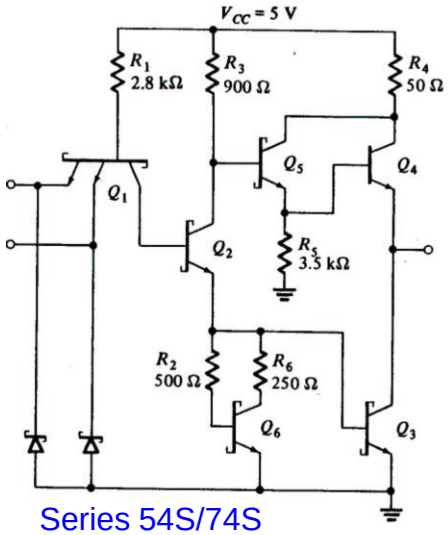
SPEEDING UP THE SWITCHING TRANSIENTS: SCHOTTKY TTL

The collector is "clamped" by a Schottky diode. This prevents the transistor reaching deep saturation.



High speed variant of TTL
Schottky transistors which have faster switching speed
Schottky-barrier diode connected from base to collector to prevent transistor from going into saturation

BASIC SCHOTTKY TTL NAND GATE



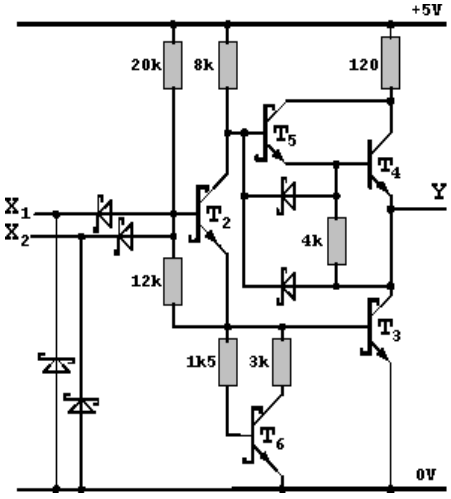
Series 54S/74S

t_{pd} = 3 nsec, P = 19 mW

Features:

Transistors: all clamped with Schottky diode except Q4 (this does not saturate)
Input diodes: high-speed clamping of input signal excursions below ground
Q5: Emitter follower to speed up 0-to-1 switching of output
50 ohm resistor: Low-to-high transient switching current reduction and impedance matching

LOW-POWER SCHOTTKY

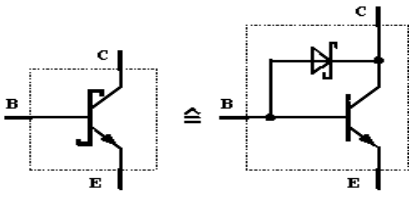


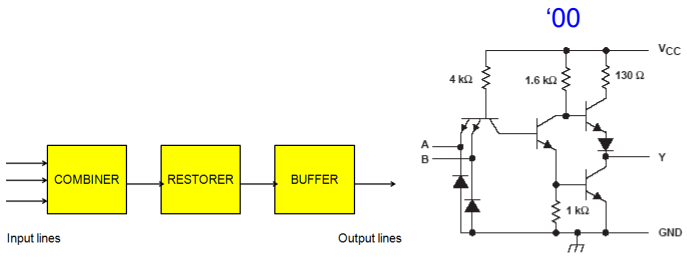
Series 54LS/74LS

t_{pd} = 9.5 nsec, P = 2 mW

Basic NAND gate with LS-(*Low-Power-Schottky*) Technology

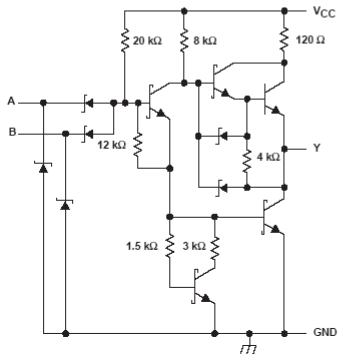
Note: input diodes NOT multi-emitter transistor



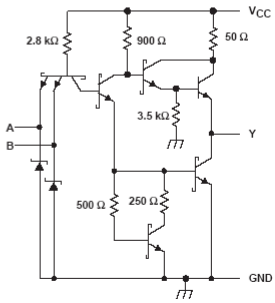


'00

'LS00



'S00



BiCMOS LOGIC

One major improvement was to combine CMOS inputs and logic and TTL drivers to form a new type of logic circuits called BiCMOS family.

In the early to late 1990s

BiCMOS technology

CMOS input structure + CMOS internal logic + Bipolar (npn transistor) output structure

high speed, high drive, low power

applications: internal bus, output interface, etc.

Common types:

BCT – BiCMOS, TTL compatible input thresholds

ABT – Advanced BiCMOS, TTL compatible input thresholds, faster than BCT

BiCMOS

BiCMOS represents an up-to-date technology.
It combines the advantages of current-controlled (BJT) and voltage-controlled devices.
It makes possible to use on one chip the optimal device and technology for each task.

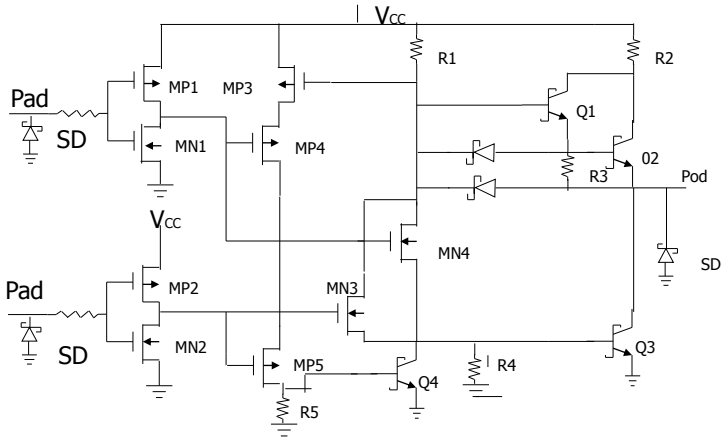
Application ⇒ VLSI & ULSI digital and mix-mode circuits.
BiCMOS is approximately 2 to 2.5 times faster than CMOS, if it is used properly. If it is not used properly, BiCMOS could be slower than CMOS and consumes more power.

E.g. the 60 MHz Intel Pentium (586) microprocessor was fabricated with 0.8 μm gate length MOS transistors in BiCMOS technology. The 2x2 cm^2 chip (270 input/output) contains more than 3 million transistors.

BiCMOS LOGIC CIRCUITS (1)

Transistor count: NMOS 4, PMOS 5, BJT 4

74BC00 NAND



BiCMOS: APPLICATION EXAMPLES

Carry look ahead in adders: the carry can be calculated from the *generate* and *propagate* combinations. Fast operation is ensured by using bipolar output stages in the implementation of

$$C_{i+1} = G_i + P_i C_i$$

allowing a fast charging of the loading capacitances.

Other example is the driving of buses, which also represent relatively large capacitive loads.

EMITTER COUPLED LOGIC (ECL)

The ECL family (also called current-mode logic, CML) is the fastest logic family in the group of bipolar logic families. The characteristic features that give this logic family its high speed or short propagation delay are outlined as follows:

1. It is a nonsaturating logic. That is, the transistors in this logic are always operated in the active region of their output characteristics. They are never driven to either cut-off or saturation, which means that logic LOW and HIGH states correspond to different states of conduction of various bipolar transistors. The main factor, limiting the switching speed of TTL type circuits, the minority carrier storage is not present or at least is very weak.

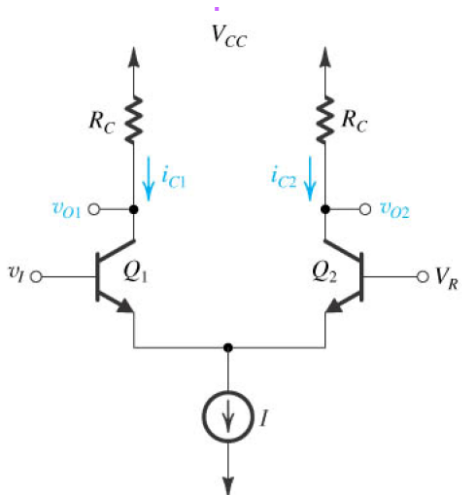
EMITTER COUPLED LOGIC (ECL)

2. The logic swing, that is, the difference in the voltage levels corresponding to logic LOW and HIGH states, is kept small (typically 0.85 V), with the result that the output capacitance needs to be charged and discharged by a relatively much smaller voltage differential.

3. The circuit currents are relatively high and the output impedance is low, with the result that the output capacitance can be charged and discharged quickly.

ECL DIFFERENTIAL PAIR

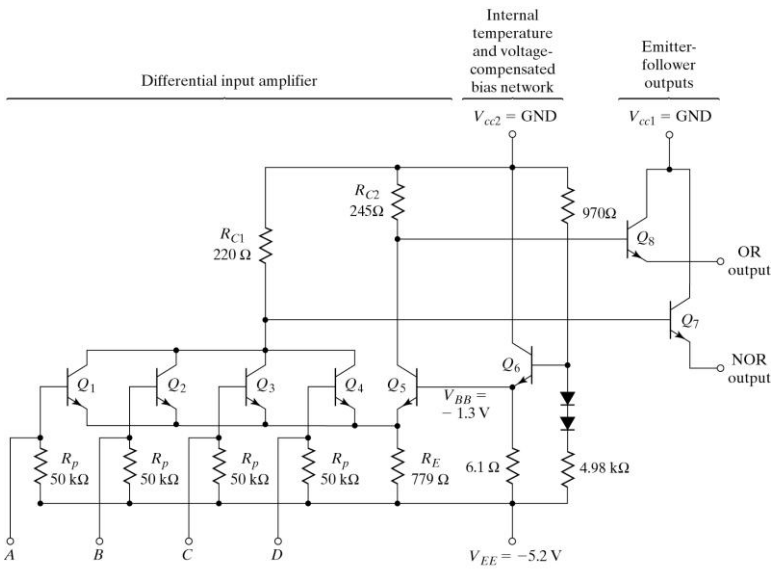
Emitter-coupled logic (ECL) is based on the use of the current-steering switch, most conveniently realised using this differential pair.



ECL FEATURES

Nonsaturated digital logic family
Propagation rate as low as 1-2 ns
Used mostly in high speed circuits
Noise immunity and power dissipation is the worst of all logic families.
High level -0.8V, Low level -1.8V
Including
- Differential input amplifier
- Internal temperature and voltage compensated bias network
- Emitter-follower outputs

ECL BASIC GATE



ECL BENEFITS

ECL gates produce both true and complemented outputs.

ECL gates are fast since it the BJTs are always in forward active mode, and it only takes a few tenths of a volt to get the output to change states, hence reducing the dynamic power.

ECL gates provide near constant power supply current for all states thereby generating less noise from the other circuits.

The ECL gate structure inherently has high input impedance and low output impedance, which is very conducive to achieving large fan-out and drive capability.

ECL PERFORMANCE

Different subfamilies of ECL logic include among others MECL-I, MECL-II, MECL-III, MECL 10K, MECL 10H and MECL 10E.

As an example the basic characteristic parameters of MECL-10H are as follows:

gate propagation delay=1 ns;
flip-flop toggle frequency=250MHz (min.);
power dissipation per gate=25 mW;
delay–power product=25 pJ.

ECL PERFORMANCE

ECL performance is illustrated with data for 4 bit 10181 type adder without and with type 10179 fast carry unit

Number of bits	Add time (ns) no fast carry chip	Total add time (ns) with fast carry chip
4	8	
8	11	
16	17	16 (1 -79, 4 -81)
24	23	17 (1 -79, 6 -81)
32	30	19 (2 -79, 8 -81)
64	54	25 (4 -79, 16 -81)

COMPARISON OF LOGIC FAMILIES

Parameter	CMOS	TTL	ECL
Basic gate	NAND/NOR	NAND	OR/NOR
Fan-out	>50	10	25
Power per gate (mW)	1 @ 1 MHz	1 - 22	4 - 55
Noise immunity	Excellent	Good	Acceptable
t_{PD} (ns)	1 - 200	1.5 – 33	1 - 4

FIGURE-OF-MERIT: POWER-DELAY PRODUCT

The product of the average power consumption and average propagation delay. Since the clock cycle is limited by the propagation delay, this number is essentially the typical energy consumption per cycle per gate.

Values are currently in the picoJoule range.

On thing that makes this a good *figure-of-merit* is that many of the simple things one can do to improve (decrease) propagation delay essentially increases (degrades) the current and thus the power consumption, so the PDP remains constant.

POWER-DELAY PRODUCT

”Good” circuit: small delay and small power dissipation.

Figure-of-merit: the product of these two parameters (power-delay product).

Standard 54/74 series: t_{pd} = 10 nsec, P = 10 mW/gate

$$P\, t_{pd} = 100 \text{ pJ}$$

Interpretation: approximately the energy needed to change the value of 1 bit.

SCHOTTKY TTL: POWER-DELAY PRODUCT

54S/74S series: t_{pd} = 3 nsec, P = 19 mW/gate

$P\ t_{pd}$ = 57 pJ

54LS/74LS series: t_{pd} = 9 nsec, P = 2 mW/gate

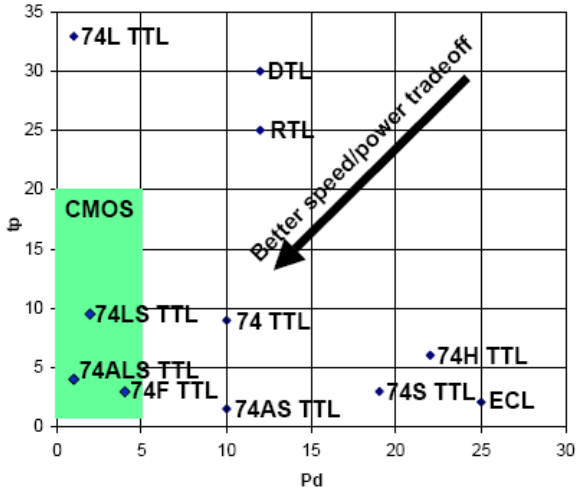
$P\ t_{pd}$ = 18 pJ

A factor of 1.5 and 5 better than standard TTL!

TTL AND CMOS: Pτ FIGURE OF MERIT

Circuit family	Propagation delay t_{pd} [ns]	Gate dissipation P_d [mW]	„Jósági" tényező P_d*t_{pd} [pJ]
74xx	10	10	100
74LSxx	9.5	2	19
74ASxx	1.5	2	13
74ALSxx	4	1.2	5
74Fxx	3	6	18
74HCxx	8	0.003	24×10^{-3}
74HCTxx	14	0.003	42×10^{-3}
74ACxx	5	0.010	50×10^{-3}
74ACTxx	5	0.010	50×10^{-3}
74AHCxx	5.5	0.003	16×10^{-3}
74AHCTxx	5	0.003	14×10^{-3}
10xxx	2	25	50
10Hxxx	1	25	25

LOGIC FAMILY TRADEOFF



Progagation delay versus power dissipation

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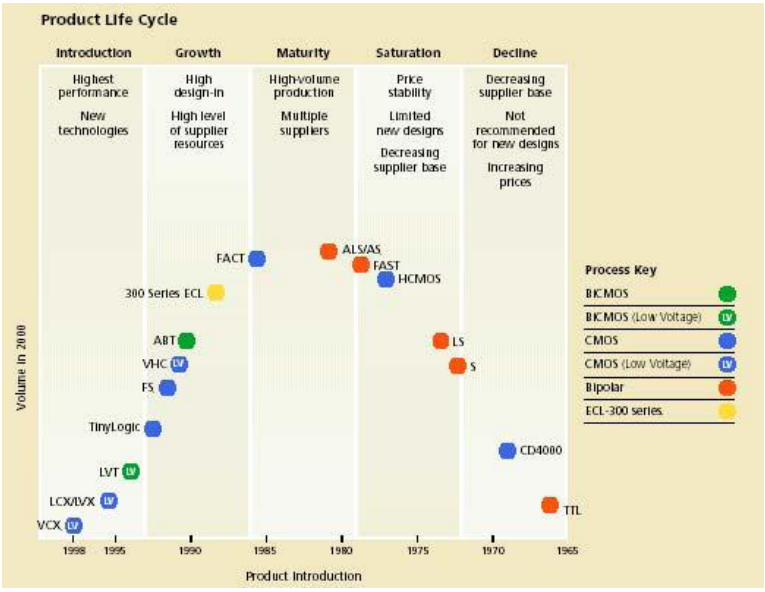
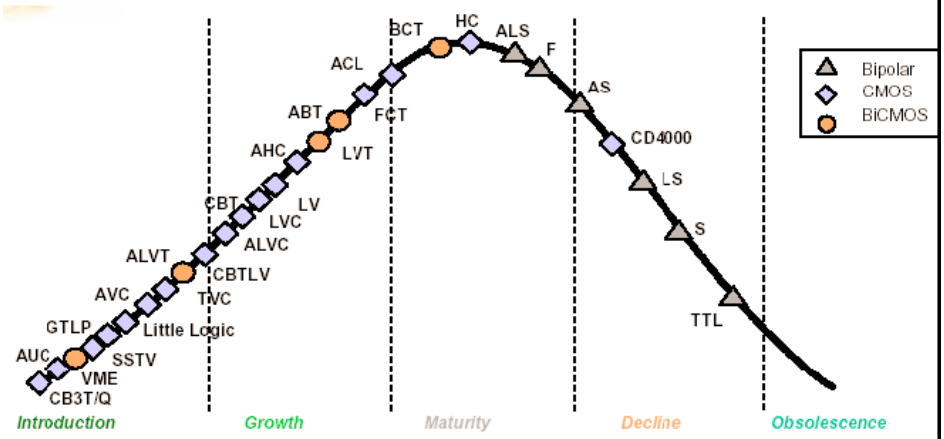
BIPOLAR AND MOS COMPARISON

Property	Bipolar	MOS
Power dissipation	medium	very small
Switching time	very small	relatively small
Input impedance	small	extremely large
Loading capability	good	very good
Noise	small	very small
Fab technology	more complex	more simple
Integration	less (in principle)	very high

LIFE CYCLE OF LOGIC CIRCUIT FAMILIES



LIFE CYCLE OF LOGIC CIRCUIT FAMILIES



REVIEW QUESTIONS

1. What do you understand by the term logic family? What is the significance of the logic family with reference to digital integrated circuits (ICs)?

2. Briefly describe propagation delay, power dissipation, speed–power product, fan-out and noise margin parameters.

3. Describe the difference between the bipolar integrated circuits and MOS integrated circuits.

4. Define and describe BiCMOS logic circuits technology and circuits. What are the advantages of a BiCMOS logic circuit?

5. Define and describe basic ECL logic. With the help of a relevant circuit schematic, briefly describe the operation of ECL OR/NOR logic. What is the advantage of ECL logic family?

REVIEW QUESTIONS

6. What are the Schottky diode and Schottky transitsor? Explain their relevance for digital logic circuits.

7. Define and explain the concept of power-delay product (PDP) of a logic gate as a figure-of-merit.