DIGITAL TECHNICS

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11. LECTURE:
TRENDS IN DIGITAL LOGIC CIRCUITS

1st (Aufumn) term 2018/2019

12. LECTURE

1. Trends in MOS and VLSI digital circuit developments

2. New device concepts:
   - Si nanowires
   - Carbon nanotube (CNT) transistors
   - Graphene transistors

DEVELOPMENT

Soon after Bardeen, Brattain, and Shockley invented a solid-state device in 1947 to replace electron vacuum tubes, the microelectronics industry and a revolution started.

Since its birth, the industry has experienced six decades of unprecedented explosive growth driven by two factors:

Noyce and *Kilby* inventing the planar integrated circuit and the advantageous characteristics that result from scaling (shrinking) solid-state devices.

CHALLENGES

Scaling solid-state devices has the peculiar property of improving cost, performance, and power, which has historically given any company with the latest technology a large competitive advantage in the market.

As a result, the microelectronics industry has driven transistor feature size scaling from 10 μm to ~30 nm during the past 50 years. During most of this time, scaling simply consisted of reducing the feature size. However, during certain periods, there were major changes as with the industry move from Si bipolar to p-channel metal-oxide semiconductor (MOS), then to n-channel MOS, and finally to complementary MOS (CMOS) planar transistors in the 1980s, which has remained the dominate technology for the past two decades.

The big challenge going forward is that the end of planar CMOS transistor scaling is near as the transistor size approaches tens of nanometers. How the industry evolves after this limit is reached is unclear.

CHALLENGES AND POSSIBLE ANSWERS

The big challenge going forward is that the end of planar CMOS transistor scaling is near as the transistor size approaches tens of nanometers. How the industry evolves after this limit is reached is unclear.

To address these challenges, present day research is focused on identifying new materials and devices that can augment and/or potentially replace the aging ~50-year-old Si transistor.

Two approaches under investigation are:
(1) nonclassical CMOS, which consists of new channel materials and/or multigate fully depleted device structures;

and

(2) alternatives to CMOS, such as *carbon based electronics*, *spintronics*, *single electron devices*, and *molecular computing*.

FUTURE

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While some of these non-Si research areas are important and will be successful in new applications and markets, it seems unlikely any of the non-Si options can replace the Si transistor for the $300 billion microelectronics industry in the foreseeable future (perhaps as long as 30 years).

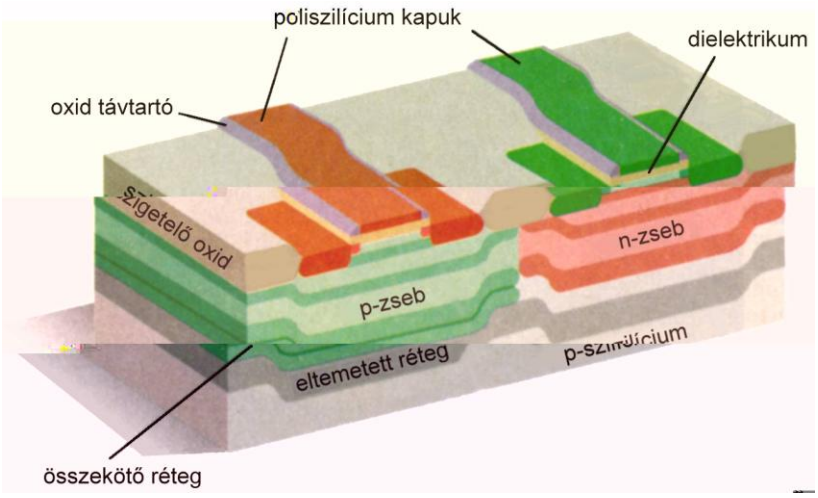
THE MOSFET AND CMOS INTEGRATED CIRCUITS

The Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) is (still) the prevailing device in microprocessors and memory circuits.

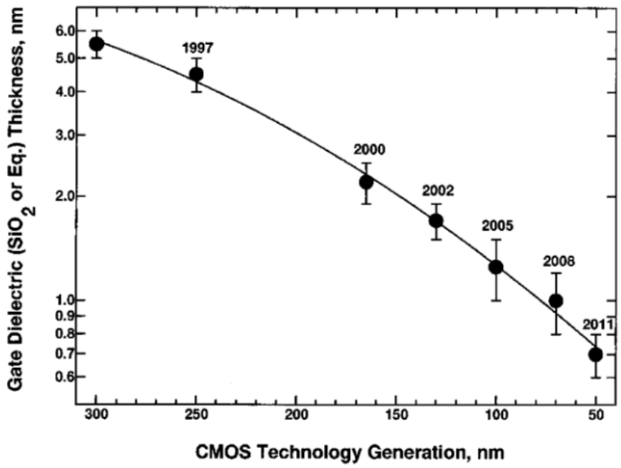
The MOSFET's advantages over other types of devices are its (i) mature fabrication technology, (ii) its successful scaling characteristics and (iii) complementary MOSFETs yielding CMOS circuits.

The fabrication process of silicon devices has evolved over the last 40 years into a mature, reproducible and reliable integrated circuit manufacturing technology.

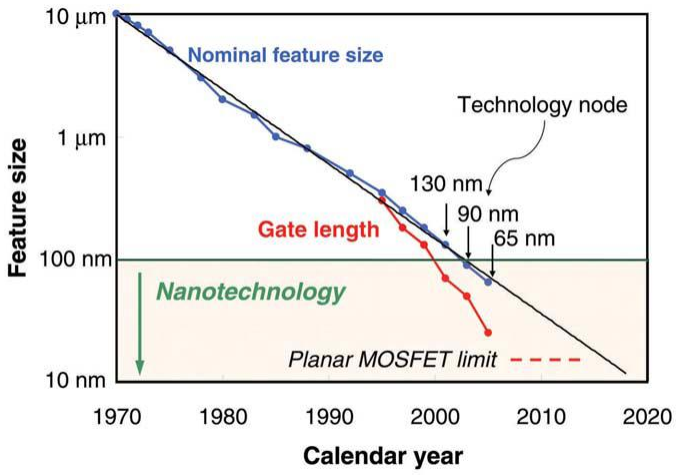
Complementary MOS, CMOS



MOS SCALING

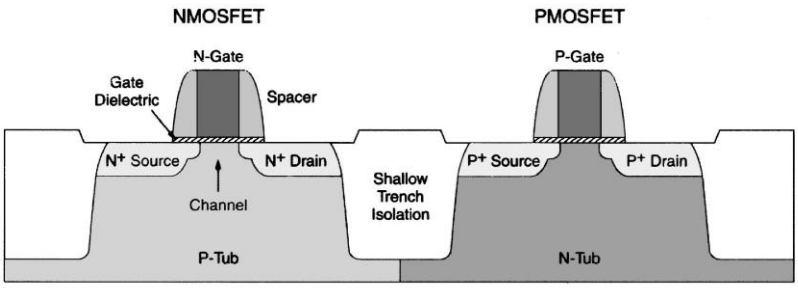


Decrease in gate SiO_2 thickness with device scaling (technology generation). Actual or expected year of implementation of each technology generation is indicated



Logic technology node and transistor gate length versus calendar year. Note mainstream Si technology is nanotechnology.

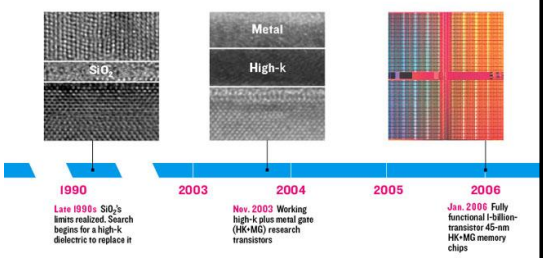
SUB-MICRON CMOS

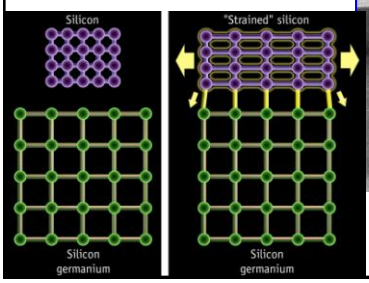


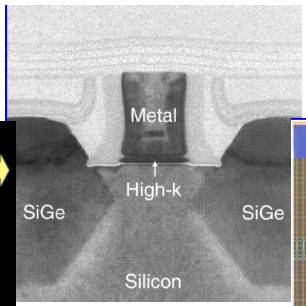
Schematic illustration of a sub-micron (channel length) CMOSFET (complementary metal–oxide–semiconductor field effect transistor) - CMOS

THE 45 nm TECHNOLOGY

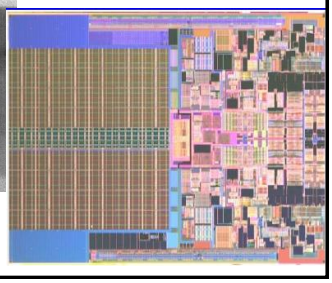
- High diel. const. HfO_2 based gate insulator in place of SiO_2
- Metal gate in place of poly-Si
- Strained Si structure (SiGe)



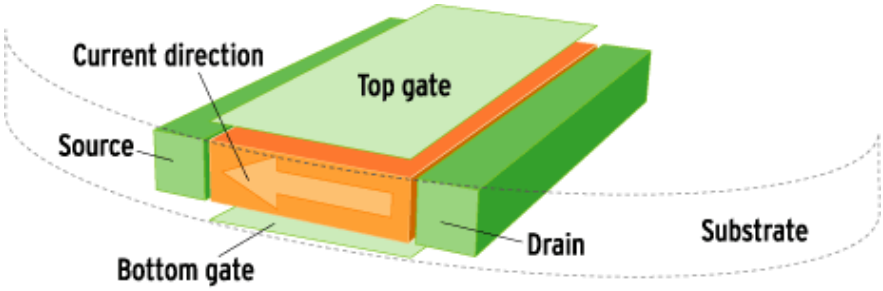




Dual core



The (final) version in the future?



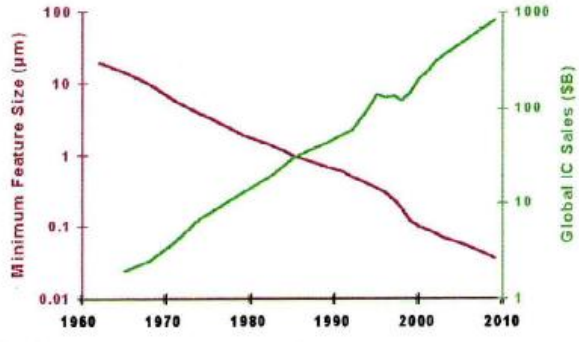
MOORE'S LAW

Gordon Moore made his famous observation in 1965, just four years after the first planar integrated circuit was discovered. In his original paper Moore predicted that the number of transistors per integrated circuit would double every 18 months.

He forecast that this trend would continue through 1975. Moore's Law has been maintained for far longer, it has become a universal law of the entire semiconductor industry. It still holds true as we enter the new century.

Moore's law is about human ingenuity not physics

MOORE'S LAW

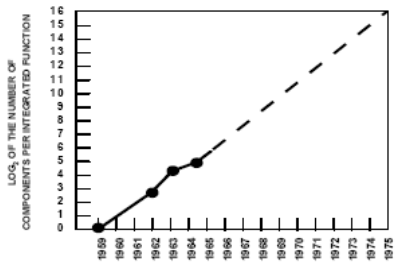


Gordon Moore (Fairchild/Intel) stated it in the1960ies, it works still in 2016 (!): 45 nm node …

Characteristic dimensions are halved in 1,8-2 year

Moore's Law

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months
- He made a prediction that semiconductor technology will double its effectiveness every 18 months



Electronics, April 19, 1965.

TECHNOLOGY SCALING

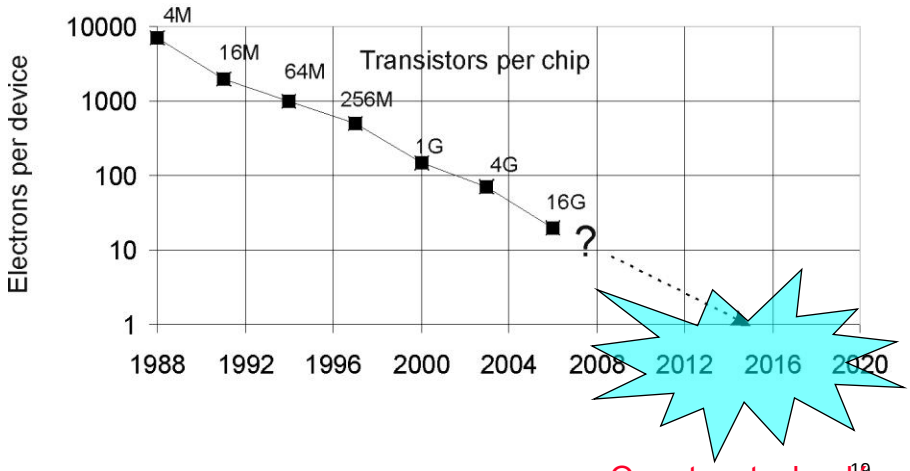
Year of Introduction	1994	1997	2000	2003	2006	2009
Channel length (μm)	0.4	0.3	0.25	0.18	0.13	0.1
Gate oxide (nm)	12	7	6	4.5	4	4
V_{DD} (V)	3.3	2.2	2.2	1.5	1.5	1.5
V_T (V)	0.7	0.7	0.7	0.6	0.6	0.6
NMOS I_{Dsat} (mA/μm) (@ $V_{GS} = V_{DD}$)	0.35	0.27	0.31	0.21	0.29	0.33
PMOS I_{Dsat} (mA/μm) (@ $V_{GS} = V_{DD}$)	0.16	0.11	0.14	0.09	0.13	0.16

Gordon Moore's "law"

: 1999, and 2001 http://public.itrs.net/

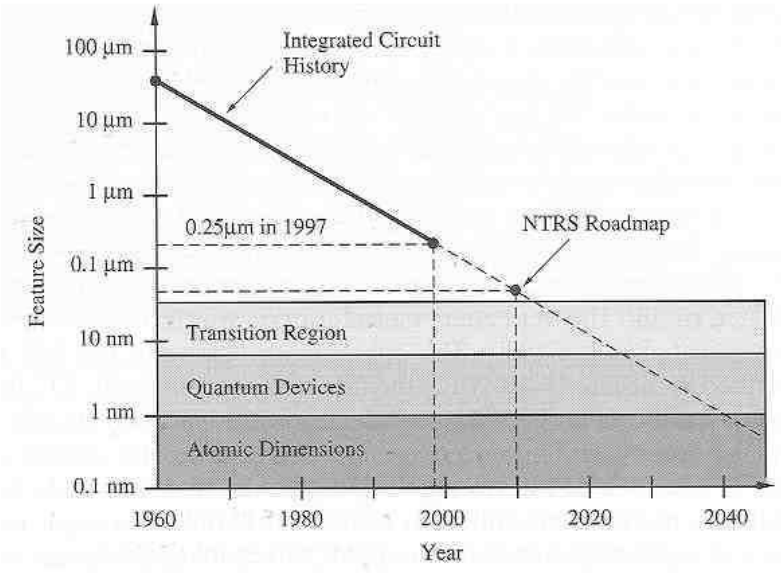
Year	2001	2005	2007	2010	2016
Half module (nm)	150	100	80	55	-
	130	80	65	45	22
Alignment accuracy	50	35	25	20	15
	46	28	23	18	9
T_{oxid} equivalent (nm)	1.6	1-1.5	1	0.8	0.5
	1.4	1.0	0.8	0.6	0.4

TOWARD THE QUANTUM LIMIT



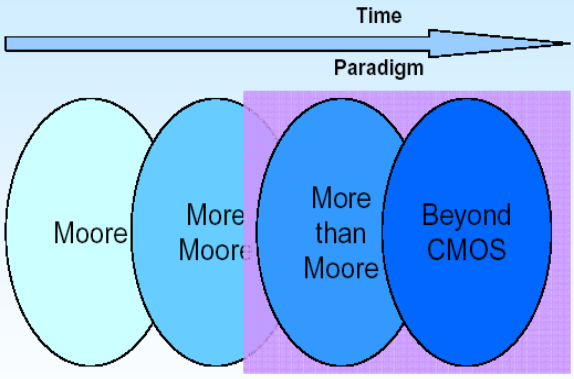
Quantum technology

MOS VLSI TRENDS



Dr. Gordon E. Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been director of the research and development laboratories since 1959.

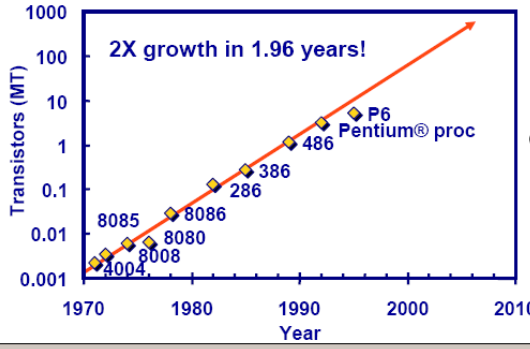
Integrate Mo(o)re



Functionalisation of Si platform
- molecular, medical, biological, hybrids...

A. Groove, R. Noyce, G. Moore, INTEL,1970

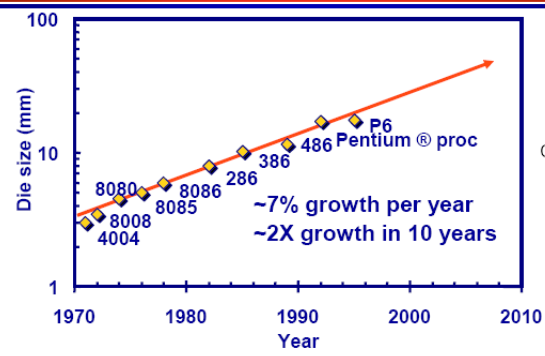
Moore's law in Microprocessors



Courtesy, Intel

Transistors on Lead Microprocessors double every 2 years

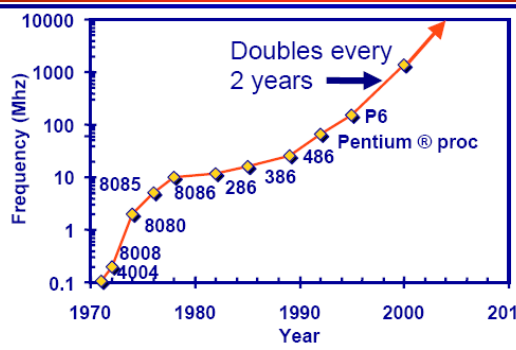
Die Size Growth



Courtesy, Intel

Die size grows by 14% to satisfy Moore's Law

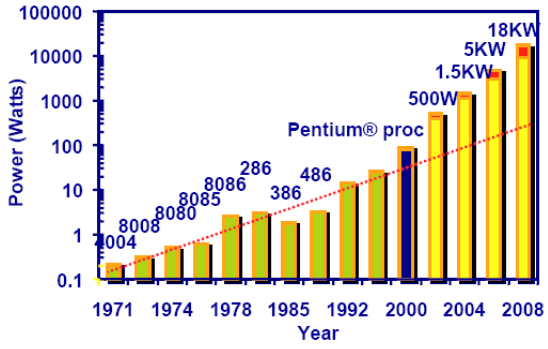
Frequency



Courtesy, Intel

Lead Microprocessors frequency doubles every 2 years

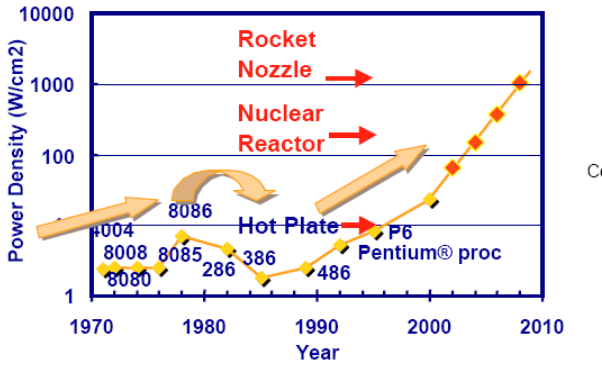
Power will be a major problem



Courtesy, Intel

Power delivery and dissipation will be prohibitive

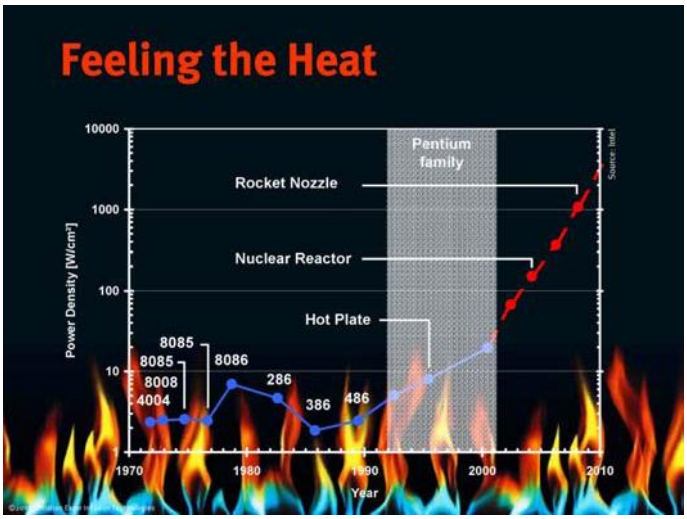
Power density



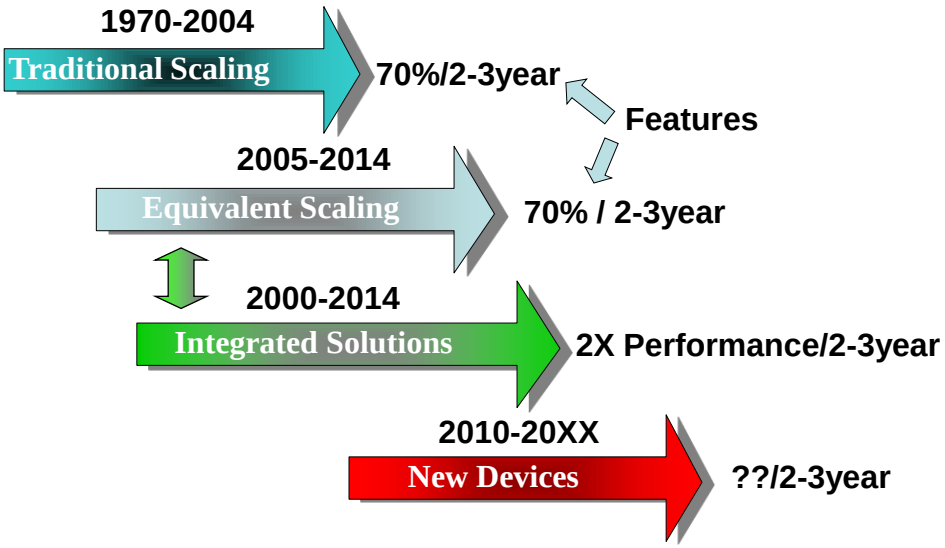
Courtesy, Intel

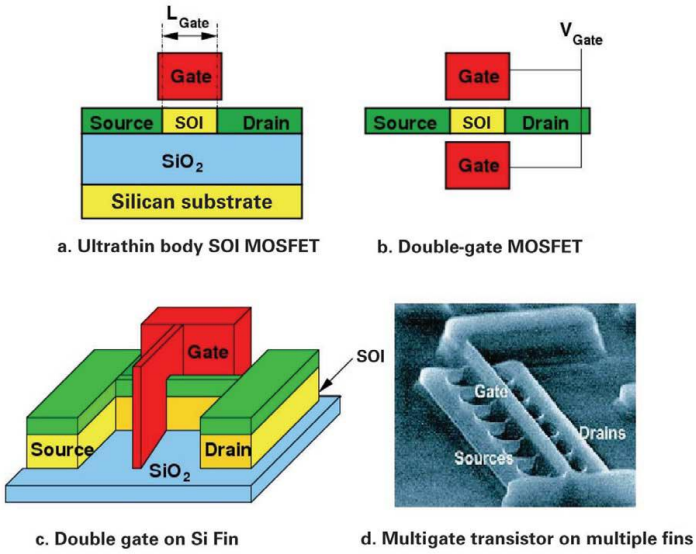
Power density too high to keep junctions at low temp

LIMITS TO FURTHER GROWTH: THE FIRE OF HELL…

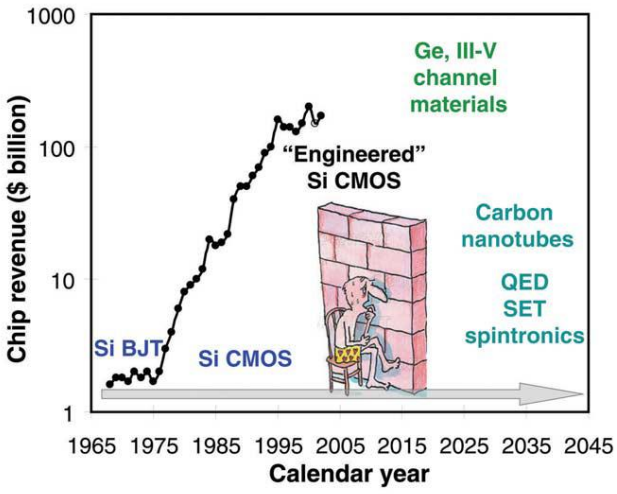


CMOS Future Directions and Beyond



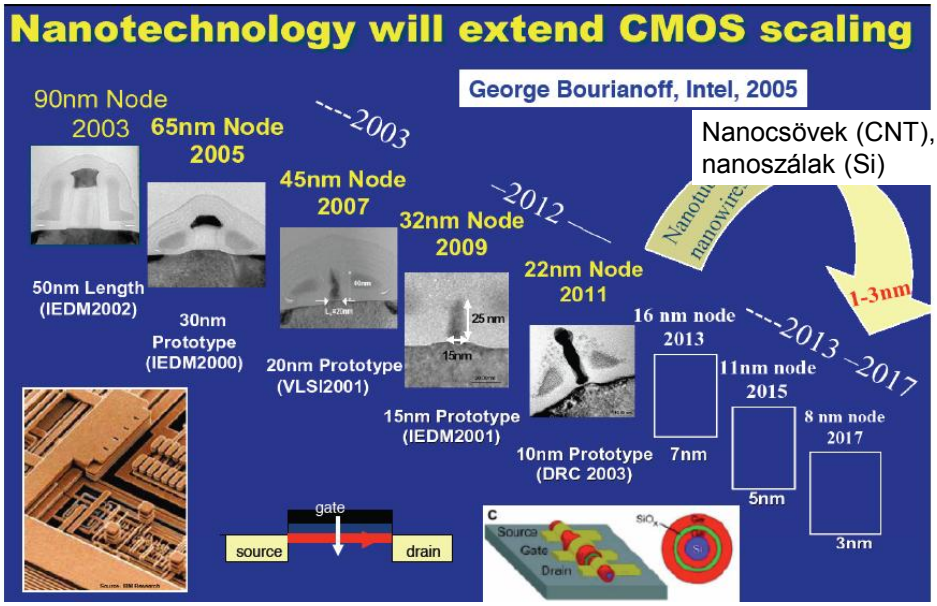


Emerging alternative fully depleted CMOS structures for continued scaling: (a) one-, (b, c) two-, and (d) three-gate fully depleted devices.

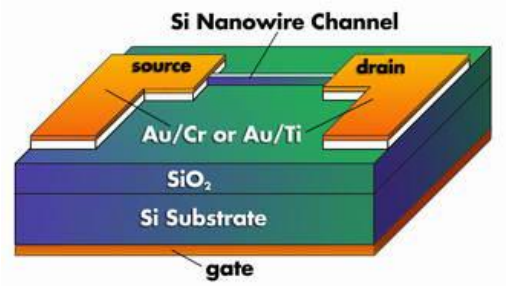


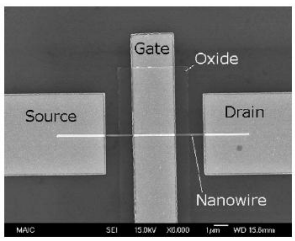
Si technology industry time line showing semiconductor revenue and the evolution of new devices and possible time frame for new device types (BJT – bipolar junction transistor, QED – quantum electronic device, and SET – single electron transistor).

ROLE OF NANOTECHNOLOGY



Si NANOWIRE TRANSISTOR





Lépték: 1 μm

Si NANOWIRE GATE-ALL-AROUND TRANSISTOR

The foremost issues are:

1. poor gate electrostatic control of the channel potential and thus degraded short-channel effects;

2. high gate leakage due to thin gate dielectric;

3. reduced channel mobility on account of increased doping in the channel; and

4. increased source/drain resistance.

These issues cause higher off-state leakage and limit the drive current leading to compromised performance, defeating the main purpose of scaling.

Solid-State Electronics 52 (2008) 1312–1317

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Si-nanowire CMOS inverter logic fabricated using gate-all-around (GAA) devices and top-down approach

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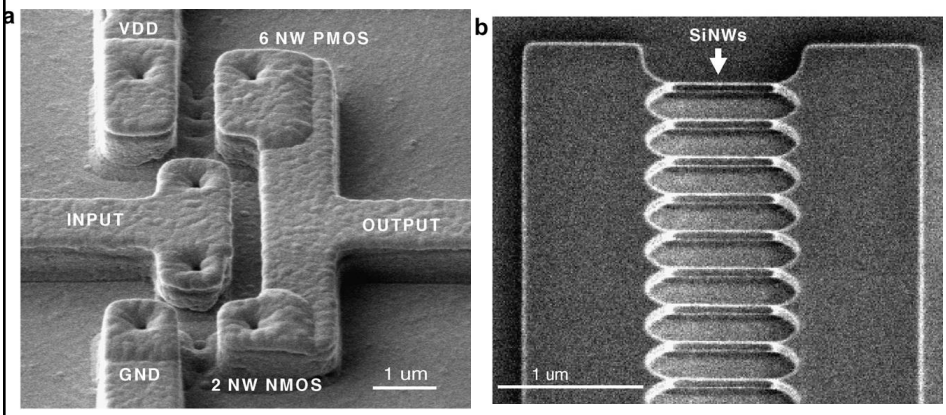
The review of this paper was arranged by Jurriaan Schmitz

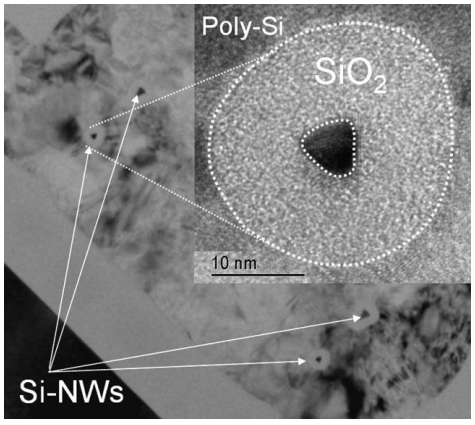
ABSTRACT

We present the monolithic integration of gate-all-around (GAA) Si-nanowire FETs into CMOS logic using top-down approach. Inverters are chosen as the test vehicles for demonstration. Empirically optimized designs show sharp ON–OFF transitions with high voltage-gains (e.g., $\Delta V_{OUT}/\Delta V_{IN}$ up to ~45) and symmetric pull-up and pull-down characteristics. The matching of the drive currents of n- and p-MOSFETs is achieved using different number of nanowire channels for N- and P-MOS transistors. The inverter maintains its good transfer characteristics and noise margins for wide range of V_{DD} tested down to 0.2 V. The detailed experimental characterization is discussed along with the electrical characteristics of the individual transistors comprising the inverter. The performances of the inverters are discussed vis-à-vis those reported in the literature using advanced non-classical device architectures such as Fin-FETs. The integration potential of GAA Si-nanowire transistors to realize CMOS circuit functionality using top-down approach is thus demonstrated.

Si NANOWIRE CMOS

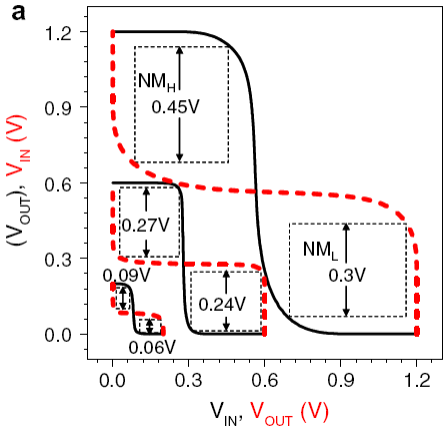


(a) SEM image of the top-down fabricated GAA Si NW inverter showing (1x2) channel N-MOS and (3x2) channel P-MOS. (b) Tilted view of multiple released nanowires in a row showing excellent yield and symmetric wires which are critical for inverter functionality.



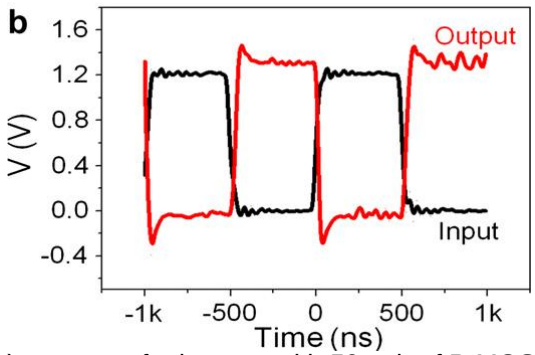
TEM image of GAA P-MOS from the inverter (1:2 N-MOS to P-MOS channel ratio). Inset on top right corner shows the enlarged image of the gate dielectric with 10 nm gate oxide surrounding the silicon NW.

INVERTER TRANSFER CHARACTERISTICS



Transfer characteristics of inverter (1:3 N-MOS to P-MOS channel ratio) at different VDD with VIN and VOUT plotted interchangeably on X- and Y-axis in a butterfly plot.

DYNAMIC RESPONSE



Dynamic (pulse) response for inverter with 50 pair of P-MOS channel and 20 pairs of N-MOS channels at 1 MHz. Output levels clearly reach VDD. The inverter delay turns out to be 64 ps for these long devices. This would scale down to 1 ps for a 20 nm node maintaining all other structural parameters and length ratios and increasing the current by a factor of five for shorter channel which is reasonable.

CARBON BASED (NANO-)ELECTRONICS

1. Carbon nanotubes (CNT) as the (near-) future (?) material of (nano-) electronics.

(According to many peoples carbon nanotubes will be the most important material of the 21th century. The future will decide whether this will come true, however the past teaches us that most prophecies did not materialize.)

2. Graphene as the as the (near-) future (?) material of (nano-) electronics.
(According to… see above point 1. …)

CNT BASED ELECTRONICS

Carbon based nanoelectronics are officially recommended by the International Technology Roadmap for Semiconductor (ITRS) in 2009 as the most promising technology for further electronics to extend the Moore law. In particular, carbon nanotube (CNT) is an exceptionally good electronic material with extremely high carrier mobility, long mean free length, and the smallest body, which may potentially bring the CNT based field-effect transistors (FETs) and integrated circuits (ICs) outstanding performances, including high speed and low power dissipation.

CNT BASED ELECTRONICS

After about 15 years development, various kinds of basic logic gates, arithmetic and control circuits have been realized on CNTs, and extensive investigations have been carried out to explore the potential advantages of CNT based electronics over Si complementary-metal-oxide-semiconductor (CMOS) technology.

CARBON BASED (NANO-)ELECTRONICS

Advantages:

High carrier mobility (fast operation, high cutoff frequency, etc.)
Exceptionally small (nano-size) dimensions (őhigh level of integration, etc.)
Good heat conduction (high-power devices, etc.)
Etc., …

CNT devices (presently in the forefront):

Wires, connections
Diode, transistor (FET)
Optoelectronic devices
Electron emitters (cold-, or field emission)

CARBON BASED (NANO-)ELECTRONICS

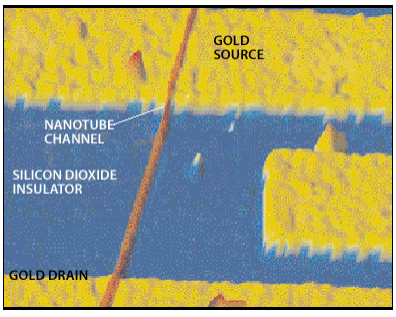
Field-effect transistors based on semiconductor *nanotubes* and *graphene nanoribbons* have already been demonstrated, and metallic nanotubes could be used as high-performance iinterconnects.

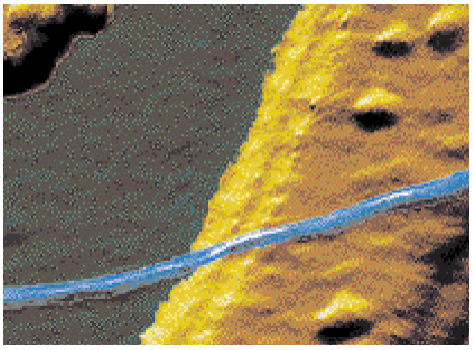
Moreover, owing to the excellent optical properties of nanotubes it could be possible to make both electronic and optoelectronic devices from the same material.

Carbon Nano Tube - CNT

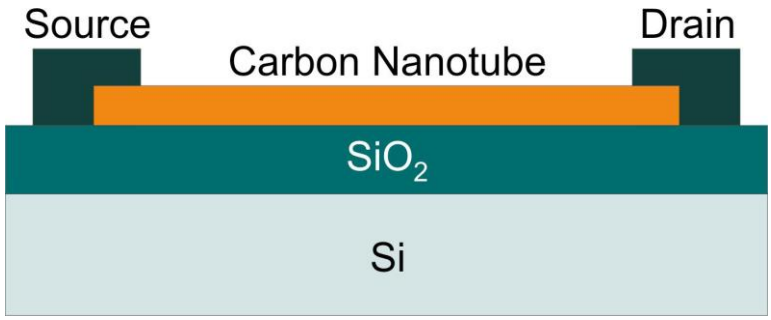
Novel materials with unique electrical and mechanical properties

Made of pure carbon, as regular and symmetric as crystals, exquisitely thin, impressively long macromolecules.





CARBON NANOTUBE FET



Schematic view of „conventional“ Carbon Nanotube Transistor

Carbon Nanotubes in Electronics

Siegmar Roth [1,2], Jiangling Wang [3], and Viera Skakalova [4]

[1] Max Planck Institut für Festkörperforschung, Stuttgart, Germany
[2] Sineurop Nanotech GmbH, Stuttgart, Germany
[3] Shanghai Yangtze Nanomaterials Co. Ltd., Shanghai, China
[4] Danubia Nanotech s.r.o., Bratislava, Slovakia

Some people claim that carbon nanotubes will be the most important material of the 21st century. The future will tell us whether this is true, but the past teaches that most predictions are wrong. In any case, carbon nanotubes certainly are the most popular material of the present: Since their discovery in 1991 [1] some 20 000 publications have appeared and some 1000 patents have been filed. Fig. 1 shows the computer model of a carbon nanotube.

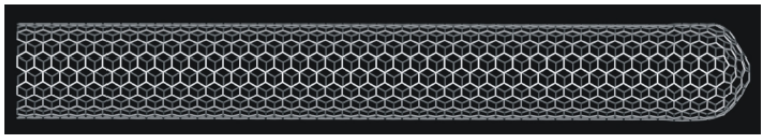


Fig. 1: Computer model of a single-walled carbon nanotube.

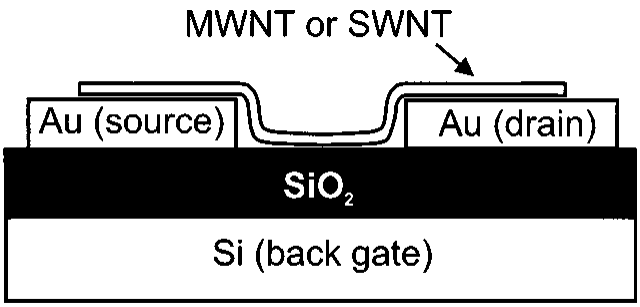
Carbon nanotubes are seamless tubes of graphitic monolayers, about 1 or 2 nanometers in diameter and up to several micrometers or even millimeters long. Depending on the diameter and on the details of seamless joining, the nanotubes are metallic or semiconducting. Because of the strong carbon-carbon bond and because of phase space arguments in narrow

CARBON NANOTUBE FET

Carbon nanotubes are a new form of carbon with unique electrical and mechanical properties. They can be considered as the result of folding graphite layers into carbon cylinders and may be composed of a single shell–single wall nanotubes, or of several shells—multi-wall nanotubes. Depending on the folding angle and the diameter, nanotubes can be metallic or semiconducting.

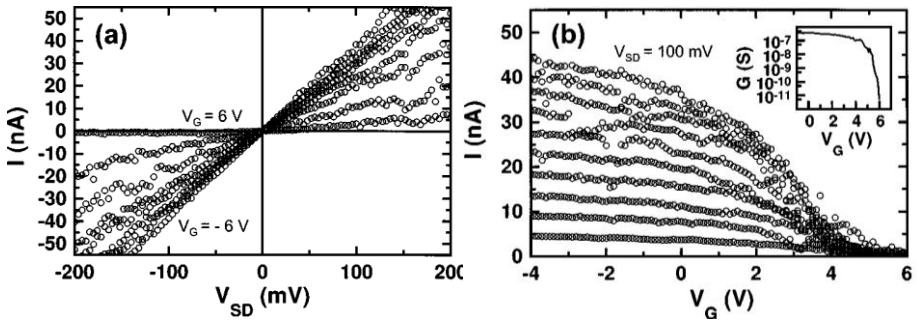
Their interesting electronic structure makes carbon nanotubes ideal candidates for novel molecular devices. Metallic NTs, for example, were utilized as Coulomb islands in single-electron transistors and, very recently, several groups built a molecular field-effect transistor (FET) with a semiconducting nanotube.

CNT FET



Schematic cross section of the FET devices. A single nanotube (NT) of either multi-wall (MW) or single-wall (SW) type bridges the gap between two gold electrodes. The silicon substrate is used as back gate.

CNT FET CHARACTERISTICS



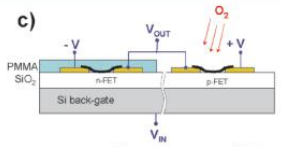
Output and transfer characteristics of a SWNT-FET: I –V_{SD} curves measured for 0, 1, 2, 3, 4, 5, and 6 V.
I –V_G curves for10– 100 mV in steps of 10 mV.
The inset shows that the gate modulates the conductance by 5 orders of magnitude.

CARBON NANOTUBE FET

Transport in the nanotubes is dominated by holes and, at room temperature, it appears to be diffusive. Using the gate electrode, the conductance of a single wall nanotube FET could be modulated by more than 5 orders of magnitude. An analysis of the transfer characteristics of the FETs suggests that the nanotubes have a higher carrier density than graphite and a hole mobility comparable to heavily p-doped silicon.

CHALMERS

Carbon nanotube inverter - 2001



Nano Letters 2001

Carbon Nanotube Inter- and Intramolecular Logic Gates

V. Derycke, R. Martel, J. Appenzeller, and Ph. Avouris*

IBM Research Division, T. J. Watson Research Center, Yorktown Heights, New York 10598

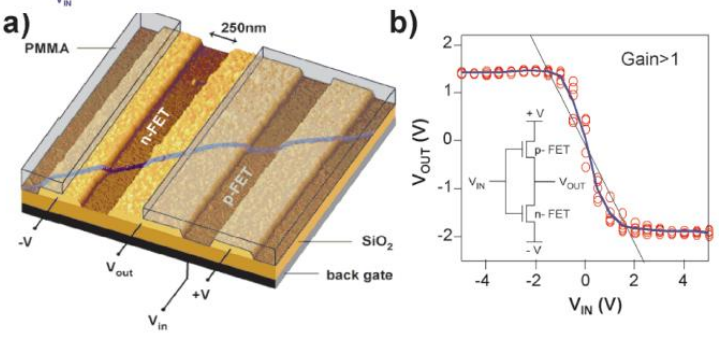
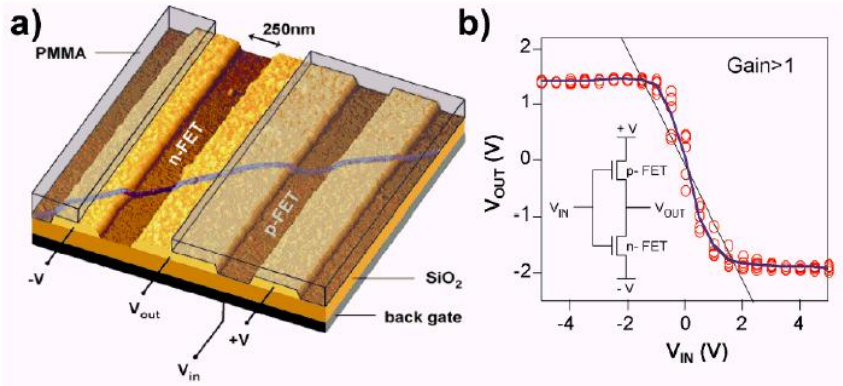


Figure 3. (a) AFM image showing the design of an intramolecular logic gate. A single nanotube bundle is positioned over the gold electrodes to produce two p-type CNTFETs in series. The device is covered by PMMA and a window is opened by e-beam lithography to expose part of the nanotube. Potassium is then evaporated through this window to produce an n-CNTFET, while the other CNTFET remains p-type. (b) Characteristics of the resulting intramolecular voltage inverter. Open red circles are raw data for five different measurements on the same device ($V = \pm 2$ V). The blue line is the average of these five measurements. The thin straight line corresponds to an output/input gain of one.

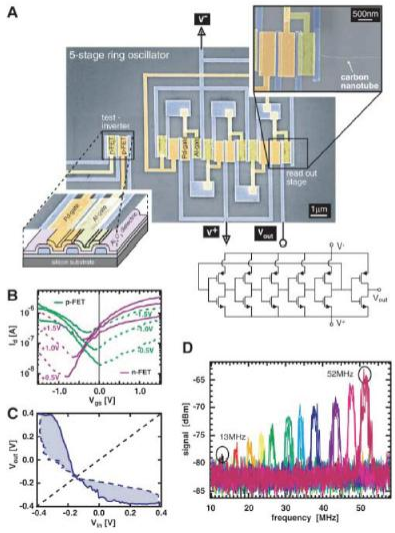
CNT FET INVERTER



The first CNTFET circuit: inverter circuit
(red circles : results of five measurement series)

CHALMERS

CNT ring oscillator - 2006



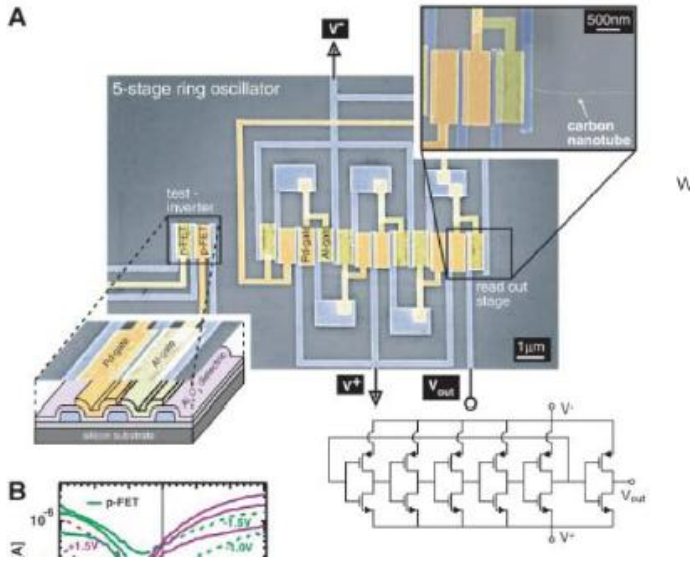
An Integrated Logic Circuit Assembled on a Single Carbon Nanotube

Zhihong Chen,[1] Joerg Appenzeller,[1]* Yu-Ming Lin,[1] Jennifer Sippel-Oakley,[2] Andrew G. Rinzler,[2] Jinyao Tang,[3] Shalom J. Wind,[4] Paul M. Solomon,[1] Phaedon Avouris[1]*

www.sciencemag.org SCIENCE VOL 311 24 MARCH 2006

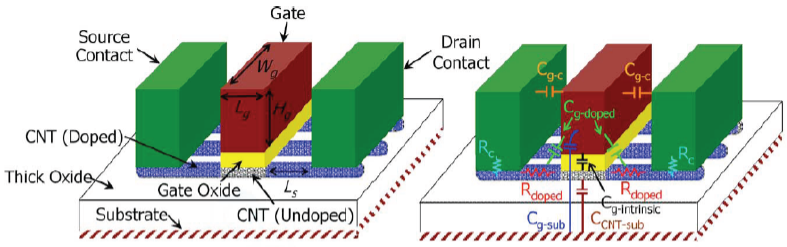
Fig. 1. (**A**) Scanning electron microscope image of a SWCNT ring oscillator consisting of five CMOS inverter stages. A test inverter was added to determine the parameter set for the actual measurement. (**B**) Characteristics for the p-type FET with Pd metal gate and n-type FET with Al gate. (**C**) Inverter characteristics and its mirrored curve. (**D**) Voltage-dependent frequency spectra. From the left to the right, the respective supply voltages are as follows: V_{dd} = 0.5 V and 0.56 V to 0.92 V (in 0.4-V increments).

CNT RING OSCILLATOR



CHALMERS

CNT FET circuits



"We have a lot to gain from CNFET-based circuits over 32 nm silicon CMOS as long as we can build circuits and architectures immune to misaligned CNTs and metallic CNTs. It is possible to design robust standard cells with guaranteed correct functionality in the presence of misaligned CNTs. We require an interdisciplinary approach to overcome the problem of metallic CNTs (e.g., to fewer than 8% metallic CNTs). We need to combine novel CNT synthesis/ selection/placement techniques, reliable ways of removing metallic CNTs after CNT growth, together with new circuit and architectural techniques to fully overcome the challenge of metallic CNTs. CNFET technology offers good scalability over silicon CMOS if CNT density can be significantly improved to 250 CNTs/*μm.*" Patil. Mitra, Wong, 2009

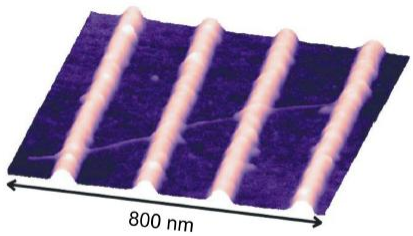
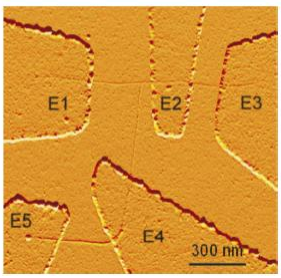


Fig. 3: AFM image of a carbon nanotube laying over 4 gold leads prepared by electron beam lithography [12].



CNT IC: SCALING DOWN

APPLIED PHYSICS LETTERS **100**, 263116 (2012)

Carbon nanotube based ultra-low voltage integrated circuits: Scaling down to 0.4 V

Li Ding,[1] Shibo Liang,[1] Tian Pei,[1] Zhiyong Zhang,[1,a)] Sheng Wang,[1] Weiwei Zhou,[2] Jie Liu,[2] and Lian-Mao Peng[1,a)]
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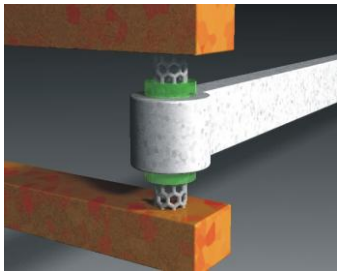
[2]*Department of Chemistry, Duke University Durham, North Carolina 27708, USA*

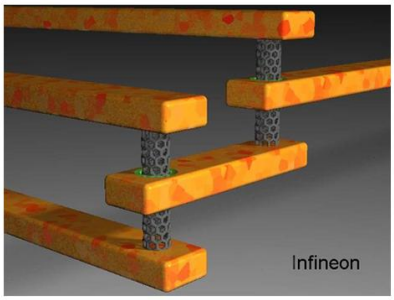
Carbon nanotube (CNT) based integrated circuits (ICs) including basic logic and arithmetic circuits were demonstrated working under a supply voltage low as 0.4 V, which is much lower than that used in conventional silicon ICs. The low limit of supply voltage of the CNT circuits is determined by the degraded noise margin originated from the process inducing threshold voltage fluctuation. The power dissipation of CNT ICs can be remarkably reduced by scaling down the supply voltage, and it is of crucial importance for the further developments of nanoelectronics ICs with higher integration density.

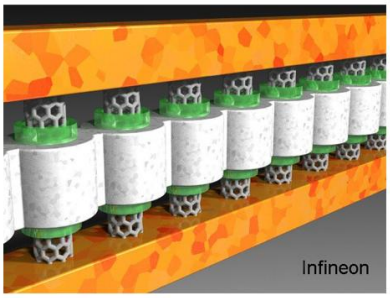
VERTICAL CNT TRANSISTOR

Vertical Nanotube Transistor
(Patented by Infineon
- and by Samsung ?!)



Integrated circuits based on semiconductor carbon nanotubes
Compatible with existing „technology”, can extend the period of validity of Moore’s law





Si AND CNT INTERCOMPARISON

	CNT FET Seidel (2004)	CNT FET Seidel (2004)	CNT FET Javey (2003)	CNT FET Javey (2004)	CNT FET McEuen (2002)	TriGate Doyle (2003)	FinFET Yu (2002)	SON Harrison (2003)
Channel Material	CNT	CNT	CNT	CNT	CNT	Si	Si	Si
Drive Voltage [V]	0.4	1.0	0.6	0.4	1.0	1.3	1.2	0.9
Drive Current [mA/μm]	15	2.4-6.4	14	11.6	2.96	0.88	0.72	0.914
Transconductance [μS/μm]	4000	2640-6430	3070	17650	6666	920	900	1170
Subthreshold Slope [mV/dec]	200	105	150-170	110	80	69.5	101	70
On Resistance [Ω/μm]	25	155-425	43	22	473	1480	1667	985
Gate Length [nm]	20	600	300	50	1400	60	10	70
Gate Oxide Thickness [nm]	12	8*	67	8	1	1.5	1.7	2
Off Current [nA/μm]	1.0	22**	1.0	600	N/A	120	20	1

GRAPHENE

The evolution of graphene-based electronic devices

Joydeep Basu[a]*, Jayanta Kumar Basu[b] and Tarun Kanti Bhattacharyya[a]

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(*Received 29 April 2010; final version received 21 July 2010*)

Successful isolation of single-layer graphene, the two-dimensional allotrope of carbon from graphite, has fuelled a lot of interest in exploring the feasibility of using it for fabrication of various electronic devices, particularly because of its exceptional electronic properties. Graphene is poised to save Moore's law by acting as a successor of silicon-based electronics. This article reviews the success story of this allotrope with a focus on the structure, properties and preparation of graphene as well as its various device applications.

Keywords: electronic device; FET; field effect; graphene; nanoelectronics

Source: *Int. J. of Smart and Nano Materials*, Aug. 2010

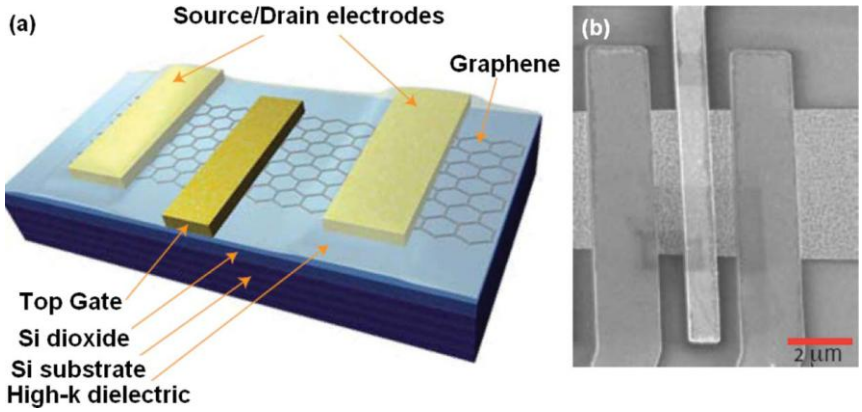
GRAPHEN ELECTRONIC DEVICES

Successful isolation of single-layer graphene, the two-dimensional allotrope of carbon from graphite, has fuelled a lot of interest in exploring the feasibility of using it for fabrication of various electronic devices, particularly because of its exceptional electronic properties.

Graphene is poised to save Moore's law by acting as a successor of silicon-based electronics.

Azért itt is érvényes, hogy a jövő eldönti, hogy ez igaz lesz-e, da a múlt arra tanít, hogy a legtöbb jóslat nem vált be…

GRAPHEN FET



A top-gated graphene field effect transistor on a SiO2/Si substrate:
(a) schematic diagram;
(b) SEM image

GRAPHENE PROPERTIES

Table 1. Comparison of the properties of graphene with those of some common semiconductors.

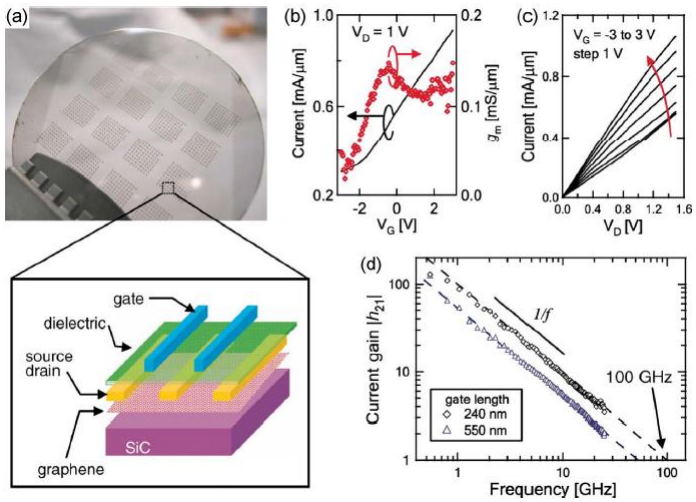
	Graphene	Si	Ge	GaAs	InAs	InP
Electron mobility ($cm^2\ V^{-1}\ s^{-1}$) @ 300 K	200,000	1400	3900	4600	16,000	2800
Band gap energy, E_g (eV)	0	1.12	0.66	1.42	0.36	1.35
Electron saturation velocity V_{sat} (10^7 cm/s)	>5	1	0.6	2.2	4.0	2.2
Density-of-states electron effective mass (m^*/m_o)	0	1.08	0.56	0.067	0.023	0.077
Relative dielectric constant, ε_r	2.4	11.9	16.0	13.1	14.6	12.4
Thermal conductivity ($W\ m^{-1}\ K^{-1}$)	5000	150	60.2	46	27	68
Lattice constant (Å)	2.46	5.43	5.65	5.65	6.06	5.87

FITTING INTO THE Si TECHNOLOGY PROCESS LINE…

Multilayered epitaxial graphene on insulating SiC substrate has been used for fabricating hundreds of transistors on a single chip. The world's first RF graphene field-effect transistor has been accomplished using 1–2 layered epitaxial graphene on SiC.

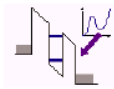
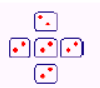
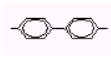
Recently, IBM has reported the creation of top-gated transistors using graphene grown on the silicon face of a 2 inch thick SiC wafer that can operate at speeds of 100 GHz with an electron carrier density of about 3×10^{12} cm^{-2} and peak mobility of 1500 $cm^2\ V^{-1}\ s^{-1}$ at room temperature.

This far surpasses the performance of the fastest GaAs transistors.



(a) Image and schematic cross-sectional view of the epitaxial graphene FETs. (b) The plot of drain current (ID) and transconductance (gm) of the device with gate voltage (VG) variation at fixed drain bias (VD) of 1 V and the source grounded. (c) The variation of ID as a function of VD for different values of VG. (d) Small-signal current gain (|h21|) variation with frequency.

NEW EMERGING LOGIC DEVICES

						
DEVICE	RESONANT TUNNELING DIODE - FET	SINGLE ELECTRON TRANSISTOR	RAPID SINGLE QUANTUM FLUX LOGIC	QUANTUM CELLULAR AUTOMATA	NANOTUBE DEVICES	MOLECULAR DEVICES
TYPES	3-Terminal	3-Terminal	Josephson Junction +Inductance Loop	-Electronic QCA -Magnetic QCA	FET	2-Terminal and 3-Terminal
ADVANTAGES	Density, Performance, RF	Density, Power, Function	High Speed, Potentially Robust, (Insenstive to Timing Error)	High Functional Density, No Interconnect in Signal Path, Fast and Low Power	Density, Power	Identity of Individual Switches (e.g., Size, Properties on Sub-nm Level. Potential Solution to Interconnect Problem
CHALLENGES	Matching of Device Properties Across Wafer	New Device and System, Dimensional Control (e.g., Room Temp Operation), Noise (Offset Charge), Lack of Drive Current	Low Temperatures, Fabrication of Complex, Dense Circuity	Limited Fan Out, Dimensional Control (Room Temperature Operation), Architecture, Feedback from Devices, Background Charge	New Device and System, Difficult Route for Fabricating Complex Circuitry	Thermal and Environmental Stability, Two Terminal Devices, Need for New Architectures
MATURITY	Demonstrated	Demonstrated	Demonstrated	Demonstrated	Demonstrated	Demonstrated

END OF LECTURE