DIGITAL TECHNICS II

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1. LECTURE:
SEQUENTIAL CIRCUITS: AN INTRODUCTION

1st year BSc course 2nd (Spring) term 2017/2018

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1. LECTURE: SEQUENTIAL CIRCUITS

1. Sequential circuits: fundamental concepts
2. Asynchronous sequential circuits
3. Synchronous sequential circuits
4. Bistable circuits, flip-flops, elementary concepts

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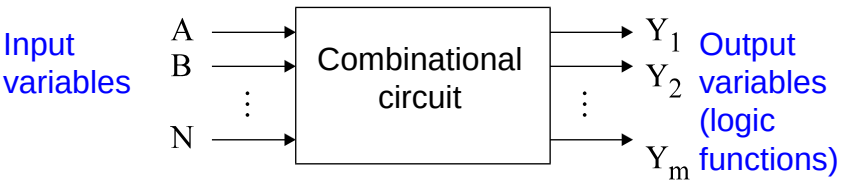
DIGITAL NETWORKS: CLASSIFICATION

Digital/logic circuits/networks can be classified into two groups:

1. Combinational logic networks
Results of an operation depend *only* on the present inputs to the operation
Uses: perform arithmetic, control data movement, compare values for decision making

2. Sequential logic networks
Results depend on both the inputs to the operation *and* the result of the previous operation
Uses: counter, controllers, etc.

COMBINATIONAL CIRCUITS: REVISION IN A NUTSHELL



$Y_i = F_i (A, B, ..., N)$ $i = 1, 2, ... M$

The combinational circuit maps an input (signal) combination to an output (signal) combination.

The same input combination always implies the very same output combination (except transients).

A combinational circuit is a circuit with no ”memory”.

SEQUENTIAL LOGIC

The combinational logic circuits have no memory. The outputs always follow the inputs.

There is an other group of circuits with a memory, which behave differently *depending upon their previous state.*
An example is the vending machine, which must remember how many and what kinds of coins have been inserted, and which behave according to not only the current coin inserted, but also upon how many and what kind of coins have been deposited previously in the given service cycle. In fact its response depends on the whole sequence of previous events.

These are referred to as sequential circuits or *finite state machines*, because they can have at most a finite number of states.

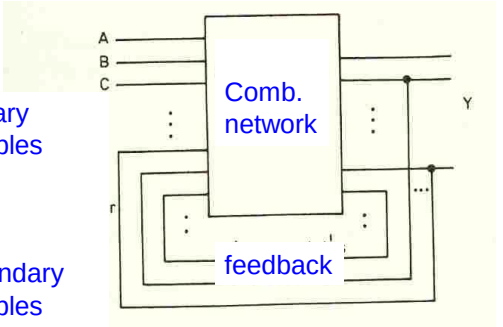
SEQUENTIAL LOGIC NETWORKS

The outputs of sequential logic networks depend not only on the actual input signal combination, but on the actual state of the network established previously. In this way the outputs depend also on the previous input signals.

Sequential logic network.

Input variables:	primary variables.
Output variables fed back:	secondary variables.

SEQUENTIAL LOGIC NETWORKS



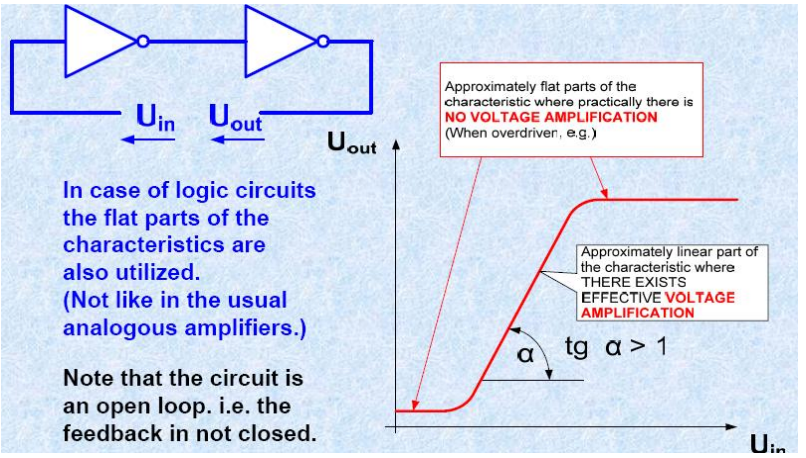
Primary variables

Secondary variables

Output variables

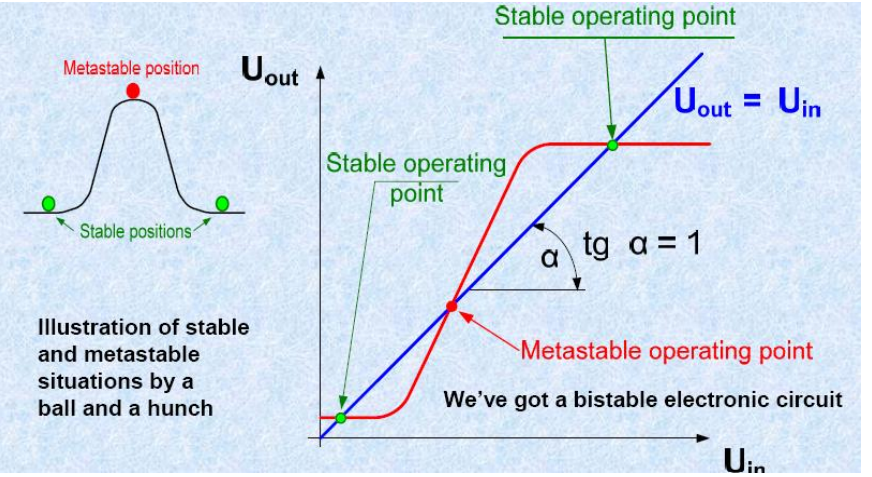
The outputs sequential logic network depend not only on the actual input signal combination, but on the actual state of the network established previously. In this way the outputs depend also on the previous input signals.
This is achieved by feedback: the output signals are feed back to the input.

LOGIC CIRCUIT WITH FEEDBACK: DISCUSSION



Analysis of the properties of a two-stage feedback amplifier feedback loop open

LOGIC CIRCUIT WITH FEEDBACK: DISCUSSION



Closing the feedback loop

PROPERTIES OF SEQUENTIAL NETWORKS

Due to the secondary variables (feedback) the sequential circuits, when excited by the same set of input signals can generate different output signals depending on what are the actual value s of the secondary signals.

These (the secondary signals) in turn depend on the sequence of previous signals arriving on the input the consequence of which that the secondary signals change their values during the operation of the system.

The name sequential logic circuit comes from this property.

The sequential circuits, in contrast to the combinational circuits have ”memory”.

”MEMORY” OF THE SEQUENTIAL CIRCUIT

It should remember those pieces of former information only which are RELEVANT to its operation.

That information is stored by its internal state.

If it has to remember finite former information only it has got finite number of internal states.

Such a sequential circuit is known as finite (sequential) automaton, or finite digital automaton. Other name is finite state machine (FSM).

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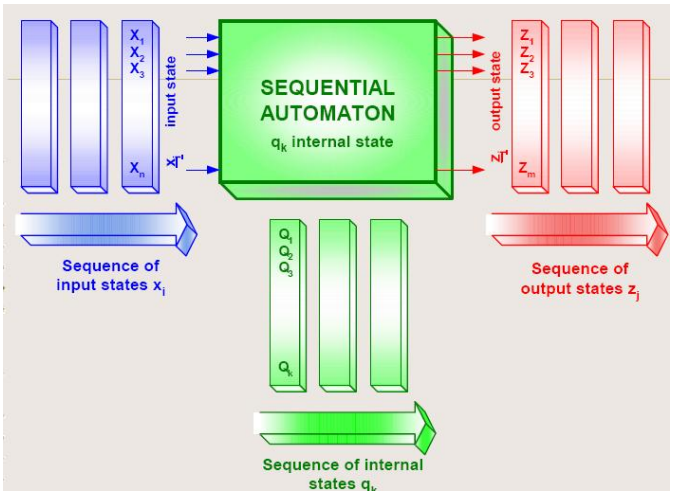
OPERATION OF A STATE MACHINE



Assuming a string of n input states to it, it generates the same length of n internal stets simultaneously it answers the control by a length n sequence of states at the output

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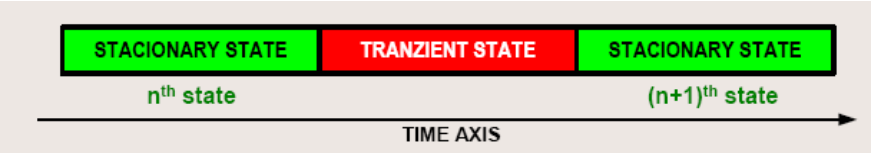
SEQUENTIAL CIRCUIT: STATIC MODEL



The static model describes the state-sequence, so called event history of the circuit, and does not describe its transients.

The time, as a variable does not occur in the functions of the states.

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ASYNCHRONOUS AND SYNCHRONOUS SEQUENTIAL NETWORKS

Sequential circuits can be classified into two groups:

1. Asynchronous sequential circuits (no synchronizing/clock signal),

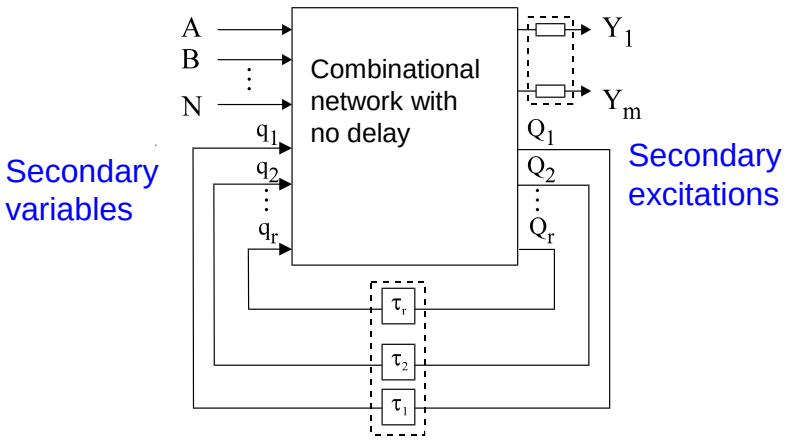
2. Synchronous sequential circuits (operating with synchronizing/clock signal).

ASYNCHRONOUS SEQUENTIAL CIRCUITS

In the asynchronous sequential circuits the inherent time delay in the feedback loop will ensure the „memory" property necessary to generate the secondary variables.

In this case the logic state transitions occur at different times, i.e. asynchronously.

ASYNCHRONOUS SEQUENTIAL CIRCUIT



The output signals are fed back to the input (secondary variables). Asynchronous operation. The key of the proper operation are the time delays in the feedback circuit.

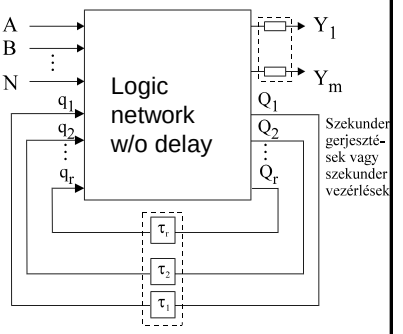
ASYNCHRONOUS SEQUENTIAL CIRCUIT

Secondary excitations are functions of the primary (input) and secondary variables

$Q_i = G_i(A, B, \ldots, N; q_1, q_2, \ldots, q_r)$

here $i = 1, 2, \ldots r$

Secondary variables

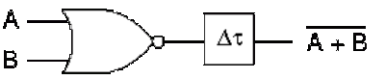


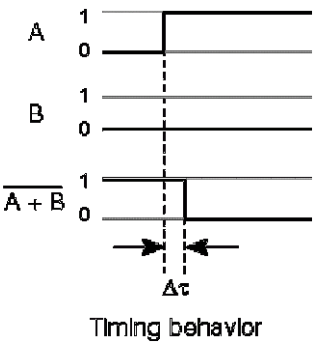
The output variables are determined by the primary (input) and secondary variables

$$Y_i = G_i(A, B, \ldots, N; q_1, q_2, \ldots, q_r)$$

here $i = 1, 2, \ldots r$

A NOR GATE WITH A LUMPED DELAY





Timing behavior

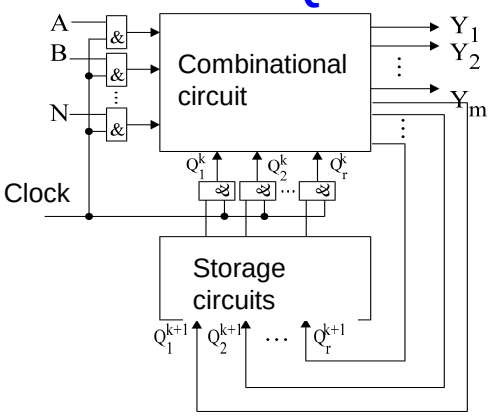
This delay between input and output is at the basis of the functioning of an important memory (storage) element, the *flip-flop*.

SYNCHRONOUS SEQUENTIAL CIRCUITS

The operation is synchronized , a separate signal is used: CLOCK PULSE, CP.

All changes occur in predetermined time (practically a short time interval), determined by the arrival of the clock signal.

SYNCHRONOUS SEQUENTIAL CIRCUIT



The output state variables are written into the storage circuits with the arrival of the clock signal. The stored signals will serve as a „memory”. They will affect the input at the arrival of the next clock signal.

OPERATION OF SYNCHRONOUS SEQUENTIAL CIRCUITS

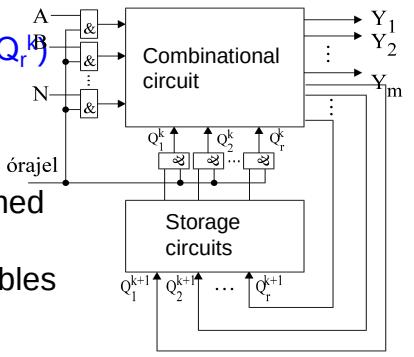
The signals feed back from the output to the input (secondary variables) do not affect the operation instantaneously, but they are written in and stored in the storage elements when the clock signal arrives. The values of these stored variables will affect the input only when the next clock signal arrives.

SYNCHRONOUS SEQUENTIAL CIRCUIT

The (k+1)th state of the feedback network is determined by the kth state of the variables and storage elements

$Q_i^{k+1} = G_i(A^k, B^k, \ldots, N^k; Q_1^k, Q_2^k, \ldots, Q_r^k)$

here i = 1, 2, … r



The output in the kth state is determined by the values of the inputs (primary variables) and of the secondary variables (internal state) valid in the kth state

$Y_i^k = F_i(A^k, B^k, \ldots, N^k; Q_1^k, Q_2^k, \ldots, Q_r^k)$

here i = 1, 2, … m

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MEALY AND MOORE MACHINES

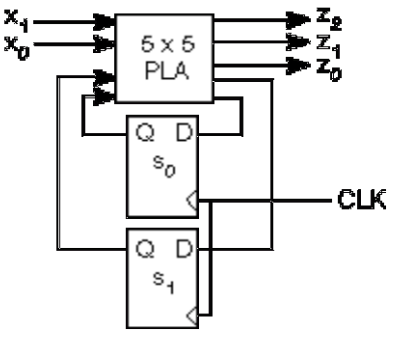
There are two types of finite state machines that can be built from sequential logic circuits:

Moore machine: the output depends only on the internal state (since the internal state only changes on a clock edge, the output also changes on a clock edge).

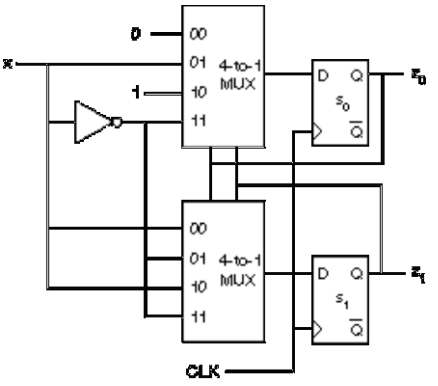
Mealy machine: the output depends not only on the internal state, but also on the inputs.

MEALY VERSUS MOORE MACHINES

Mealy Model: Outputs are functions of Inputs and Present State.

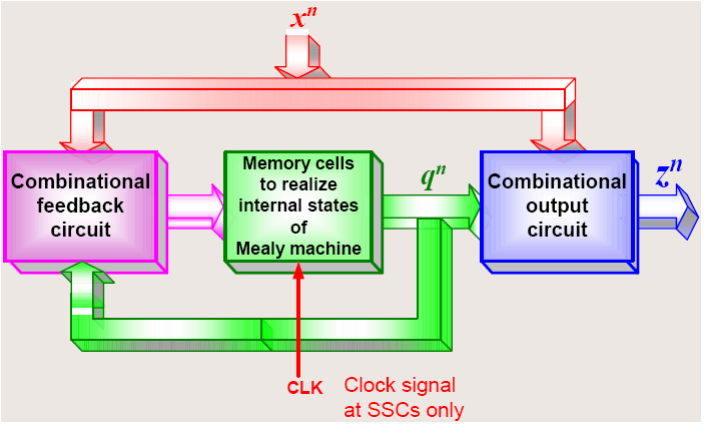


- Moore Model: Outputs are functions of Present State only.



Both are equally powerful.

LOGIC STRUCTURE OF MEALY MACHINE



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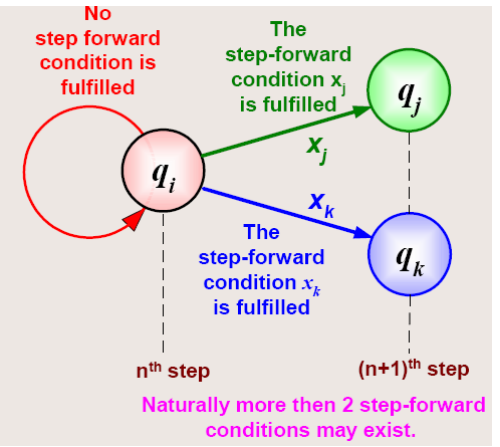
STATE TRANSITION DIAGRAM (STATE GRAPH)



The state transition diagram (state graph) is used to describe the behaviour of sequential circuits. It consists of nodes, and directed lines (edges) connecting them.

Node: the internal state of the network.

Edge: transition from a state to an other one under the action of a given input combination.

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STATE TRANSITIONS OF THE MEALY MACHINE

The internal states of a Mealy machine can be very well represented by the nodes of a so called state graph or state transition diagram and its state transitions by the directed edges of the same state graph.

This method of description will be used throughout in the analysis and synthesis of sequential circuits, e.g. in the case of flip-flops, counters, registers, etc.

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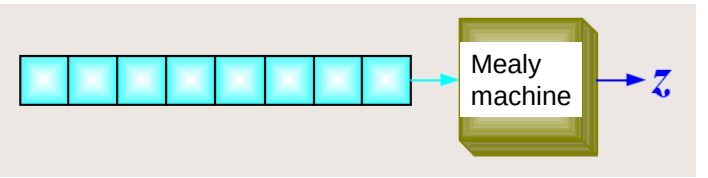
EXAMPLE: PARITY CHECKER

The task of a sequential circuit be the determination of the parity of bit of an 8-bit (series) code word.



Whatever number of bits were applied to its input it must remember only the parity of the bits already applied, i.e. whether it is even or odd.
To remember those two choices it is enough to have two internal states only and when a new bit is applied to its input it has to examine if that new bit changes the stored parity or not.

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EXAMPLE: HAMMING WEIGHT OF A CODE WORD

Let us consider now a circuit which is to determine the Hamming weight of an 8 bit (serial) codeword. This situation is entirely different from the one in the former example, for the Hamming weight can be anything from 0 through 8.

The circuit must know in the nth step what was the Hamming weight of that part of codeword which has been received already and depending up on the particular value of bit n the circuit either increase the stored data by 1 or let it be as it is.

This case differs essentially from the case of the parity checker and it does need 8 internal states.

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ILLUSTRATION: VENDING MACHINE

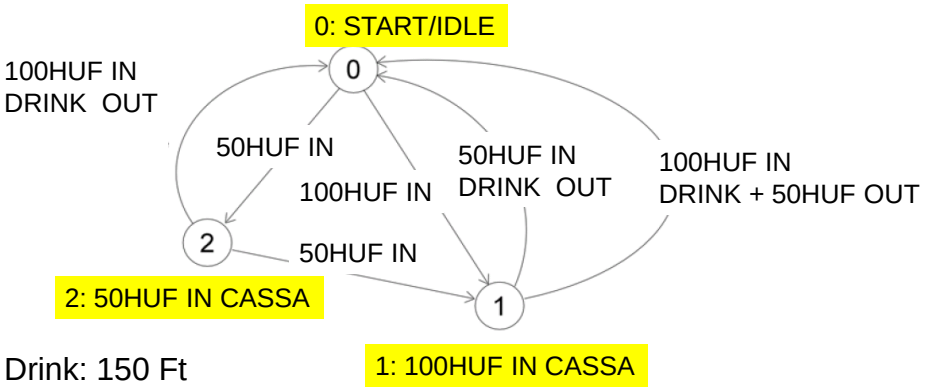
E.g. a bottled drink vending machine should ”remember” how many and what kind of coins have already been inserted into it. The ”response” of the machine depends not only on the coin last inserted, but also on how many and what kind of coins it accepted already in the given service cycle.

In fact its response depends on the whole sequence of previous events.

Example:

machine vends bottled drink for 150 HUF
it accepts coins of 50 HUF and 100 HUF
outputs drink or drink and change as appropriate

EXAMPLE: DESCRIPTION OF STATES OF A DRINK VENDING MACHINE



Drink: 150 Ft
Coin: 50 or 100 Ft

Number of states: 3 (START/IDLE, 50HUF IN CASSA, 100HUF IN CASSA)

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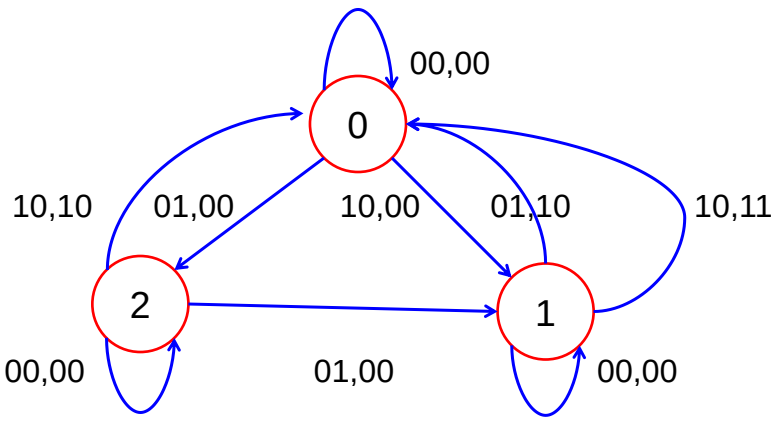
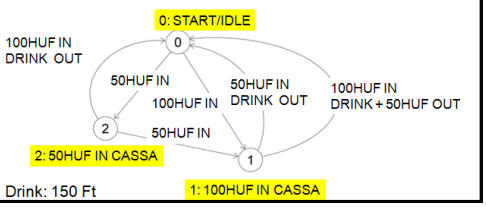
VENDING MACHINE: STATE TRANSITION DIAGRAM

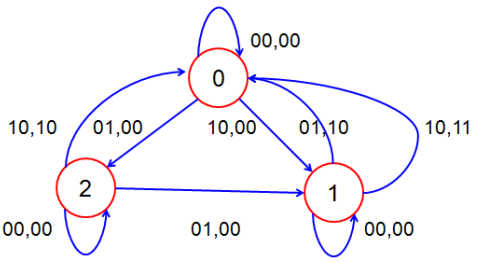


x1 – 100Ft, x0 – 50 Ft
z1 – drink out, z0 – 50 Ft out



VENDING MACHINE: STATE (TRANSITION) TABLE

100/50 Ft in (x1x0)	0 0	0 1	1 0	1 1
State (previous)	State (next)			
0 (0 Ft)	0	2	1	X
1 (100 Ft)	1	0	0	X
2 (50 Ft)	2	1	0	X



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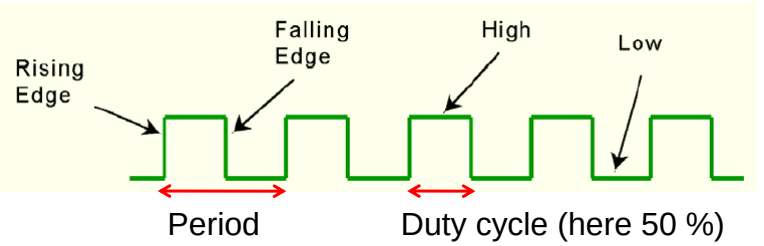
CLOCKS

A sequential circuit uses past inputs to determine present outputs: event ordering.
Clock: circuit emitting a series of pulses with precise pulse width and repetition rate.
Synchronous sequential circuit: uses clock to decide when to update the state of the circuit.



Most sequential circuits are edge triggered: they change their state on either rising or the falling edge of the pulse.

ROLE OF CLOCKS IN DIGTAL SYSTEMS

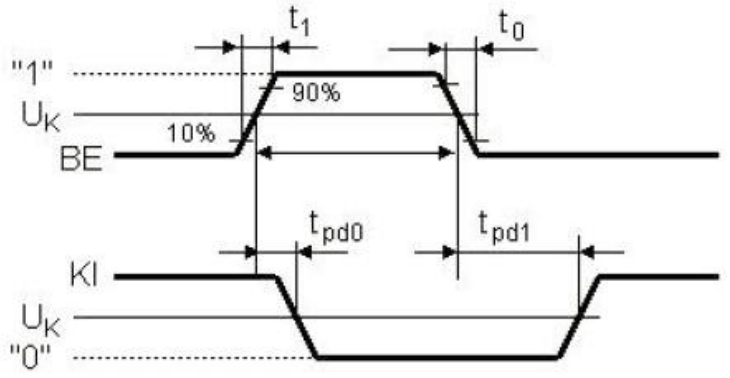
We will soon get used to the idea of a clock as an essential element of digital circuitry. When we speak of a clock signal, we mean a sequence of evenly spaced digital high and low signals proceeding at a fixed frequency. That is, the clock is a continuous sequence of square wave pulses.

There are a number of reasons for the importance of the clock. Clearly it is essential for doing any kind of counting or timing operation. But, its most important role is in providing *synchronization* to the digital circuit. Each clock pulse may represent the transition to a new digital state of a so-called ”state machine” (simple processor) we will soon encounter. Or a clock pulse may correspond to the movement of a bit of data from one location in memory to another.

ROLE OF CLOCKS IN DIGTAL SYSTEMS

A digital circuit coordinates these various functions by the synchronization provided by a single clock signal which is shared throughout the circuit. A more sophisticated example of this concept is the clock of a computer, which we have come to associate with processing speed (*e.g.* 330 MHz for typical current generation commercial processors).

CLOCK SIGNAL: DYNAMICS



Rise time: 10 % → 90 % signal level
Fall time: 90 % → 10 % signal level
Delay: between 50 % signal levels

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SIGNAL RISE AND FALL TIMES

One time constant model (e.g. RC delay)

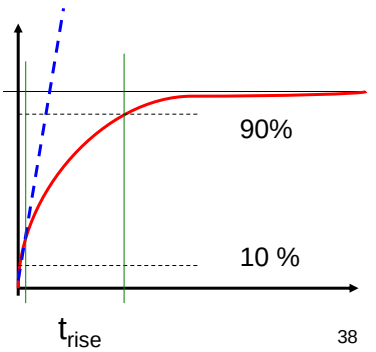
$U(t) = U_o (1 – \exp(-t/\tau))$

Time constant $\tau = RC$

$t_{rise} = \ln (0.9/0.1)\ \tau = 2.2\ \tau$

E.g. TTL type 7400 NAND gate

Load: few pF, say 5 pF, output resistance 130 ohm,
t_{rise} 1-2 nsec (gate delay is about 15 nsec).



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ELEMENTARY SEQUENTIAL CIRCUITS

Combinational networks: can be constructed from elementary combinational circuits i.e. form gates.

Sequential (synchronous and asynchronous) networks: can be constructed from elementary sequential circuits.

Elementary sequential circuits: left alone, the have only one they can handle only very simple logic tasks, they have only one secondary (state) variable. Therefore they have only two states and one or two control inputs.

Usual names: bistable (multivibrator), memory/storage element, flip-flop.

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FLIP-FLOPS

Flip-flop, *latch* or *bistable multivibrator* is an electronic circuit which has two stable states. It is capable to function as a memory.

A flip-flop is controlled by one or two control signals and/or a gate or clock signal. The output often includes the complement as well as the normal output.

Sometimes they have separate auxiliary clear and load/set/preset inputs too.

FLIP-FLOPS: ELECTRONICS

Flip-lops are circuits that can be found in two stable balanced states (circuit values i.e. voltages, currents) do not change. Stable either permanently (change only due to an external pulse) or temporarily (after a certain time change into other state spontaneously).

The circuit state when the voltages are changing is called non-stable.

Flip-fops can be divided into the following groups, according to the character of the stable balanced states:
bistable (both states are permanently stable),
monostable (often called one-shots) (one of the states is permanently stable, the other one is stable only temporarily),
astable (both states are temporarily stable).

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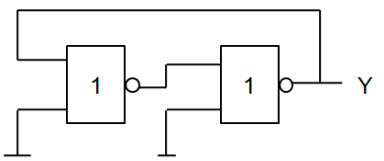
FLIP-FLOPS: ELECTRONICS

The basis for the flip-flops is an amplifier with a positive feedback (pair of simple transistor amplifying stages, or one amplifying stage and a transformer for creating the positive feedback, etc.).



In digital technique a pair of inverters or logical elements with similar behaviour are often used.
This circuit can have two stable states, either Y = 0 or Y = 1.

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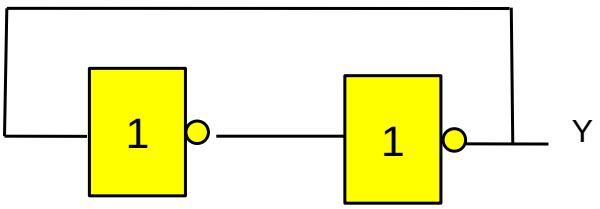
TWO INVERTERS WITH FEEDBACK



This circuit can have two stable states, either Y = 0 or Y = 1. However its state cannot be set or controlled by external logic signal(s).

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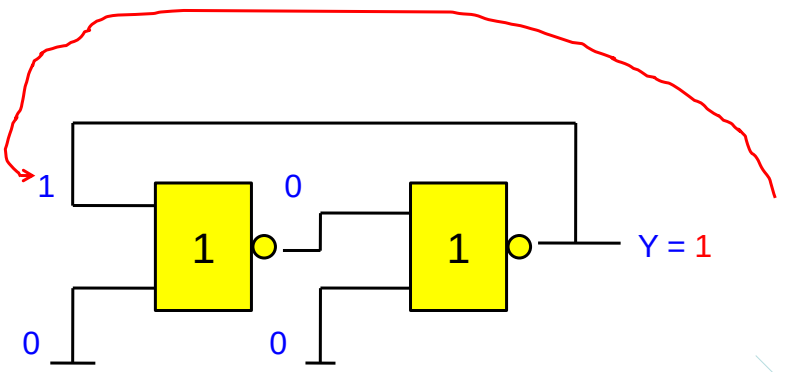
LOGIC CIRCUIT WITH FEEDBACK



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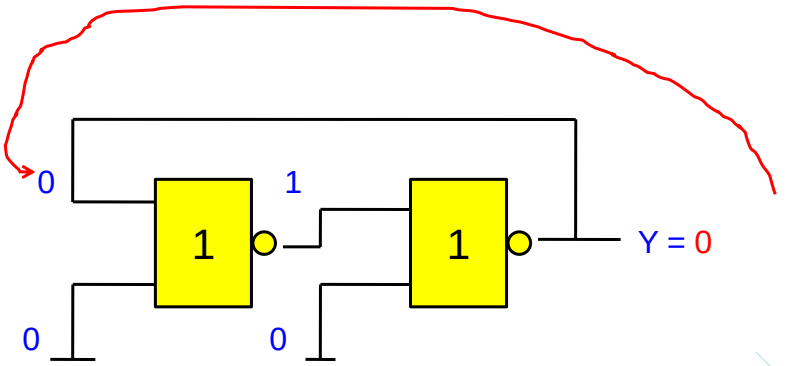
LOGIC CIRCUIT WITH FEEDBACK



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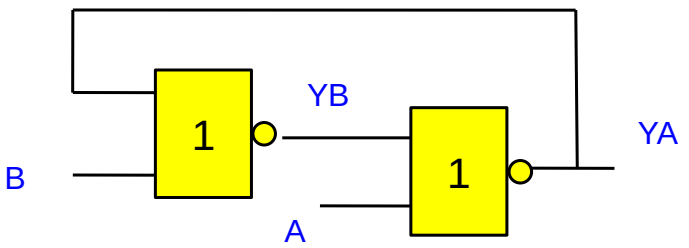
TWO NOR GATES WITH FEEDBACK

Inputs: **A**, **B**, outputs: **YA**, **YB**



Using NOR gates in place of inverters, the circuit‘s state (output(s)) can be controlled by appropriately setting the inputs.

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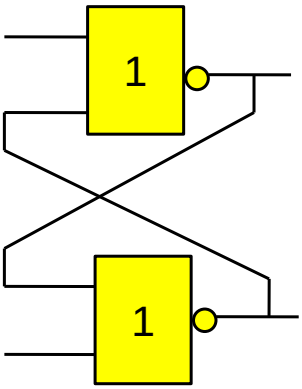
TWO NOR GATES WITH FEEDBACK



Using NOR gates in place of inverters, the circuit's state (output(s)) can be controlled by appropriately setting the inputs.

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LOGIC CIRCUIT WITH FEEDBACK: DISCUSSION

Network with two stable states (bistable).

"Classic" RS flip-flop

In this case both control inputs are on 0 level, the circuit holds the state which was established by chance during switch on.

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REVISION QUESTIONS

1. What do you mean by sequential circuit? Explain with the help of a block diagram.

2. Give the comparison and explain the difference between combinational and circuits.

3. Give the comparison and explain the differences between synchronous and asynchronous sequential circuits.

4. What is the difference between a level-triggered clock and an edge-triggered clock?

REVISION QUESTIONS

5. (Combinational versus sequential circuits). Which of the following contain circuits that are likely to be combinational and which contain sequential circuits? For three cases selected give a few sentence explanation and discussion of your answer.
(a) A washing machine that sequences through the soak, wash, and spin cycles for preset periods of time.
(b) A circuit that divides two 2-bit numbers to yield a quotient and a remainder.
(c) A machine that takes a dollar bill and gives three quarters, two dimes, and a nickel in change, one at a time through a single coin change slot.
(d) A digital alarm clock that generates an alarm when a preset time has been reached.

REVISION QUESTIONS

5. (Cont.)
(e) A circuit that takes as input two decimal numbers in the range from 0 to 9, outputs a 0 if they are different, and a 1 if they are identical.
(f) A circuit that turns on or off a hall light based on the configuration of two input switches. If both Switches are in the same position, the light is off. If they are in different positions the light is on.
(g) A circuit that takes a sequence of bits, one bit at a time, and outputs a 0 or 1 after each bit that indicates if the number of is in the sequence seen so far is even or odd, respectively.
(h) A circuit with two binary inputs and four binary outputs that works as follows. The binary input indicates which of the four outputs should be driven to a 1 with the other outputs set to 0.

PROBLEMS AND EXERCISES

1. In a complete state machine, all possible transitions between states of a finite state machine (FSM) should be specified. Your state machine has two inputs, and B, and two states, S0 AND s1. You are told that your FSM behaves as follows:

The FSM moves from S0 to S1 if and only id A = 1.
The FSM moves from S1 to S0 if and only if A = 0 and B = 1.

Draw the complete state transition diagram of your FSM.