DIGITAL TECHNICS II

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2. LECTURE: ELEMENTARY SEQUENTIAL CIRCUITS: FLIP-FLOPS

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SYNCHRONOUS SEQUENTIAL LOGIC

Nearly all sequential logic today is „clocked” or „synchronous logic”: there is a „clock” signal, and all internal memory (the internal state) changes only on a clock edge. The basic storage element in sequential logic is the *flip-flop*.

The main advantage of synchronous logic is its simplicity. Every operation in the circuit must be completed inside a fixed interval of time between two clock pulses, called a “clock cycle”. As long this condition is met (ignoring certain other details), the circuit is guaranteed to be reliable.

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SYNCHRONOUS SEQUENTIAL LOGIC

Synchronous logic has two main disadvantages, as follows.
1. The clock signal must be distributed to every flip-flop in the circuit. As the clock is usually a high-frequency signal, this causes power dissipation – in other words, heat. Even the flip-flops that are doing nothing consume a small amount of power, thereby generating waste heat.
2. The maximum possible clock rate is determined by the slowest logic path in the circuit, otherwise known as the critical path. This means that every logical calculation, from the simplest to the most complex, must complete in one clock cycle. One way around this limitation is to split complex operations into several simple operations, a technique known as “pipelining”. This technique is prominent within *microprocessor* design, and helps to improve the *clock rate* of modern processors.

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ASYNCHRONOUS SEQUENTIAL LOGIC

Asynchronous sequential logic is the most general kind of sequential logic, but because of its flexibility it is also most difficult to design. The basic storage element in asynchronous logic is the *latch* (RS flip-flop). Latches can change state at any time, depending on the transitions of other signals which may themselves be produced by other latches. The complexity of asynchronous circuits tends to rise very rapidly as the number of logic gates increases, so they tend to be used mostly in smaller applications. However computer-aided design (CAD) tools are appearing that can simplify the task, and permit more complex designs.

It is of course possible to build mixed circuits containing synchronous flip-flops and asynchronous latches.

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ELEMENTARY SEQUENTIAL CIRCUITS: FLIP-FLOPS

Combinational networks: can be constructed from elementary combinational circuits i.e. form gates.
Sequential (synchronous and asynchronous) networks: can be constructed from elementary sequential circuits.

Elementary sequential circuits: *Flip-flop*, *latch* or *bistable multivibrator* is an electronic circuit which has two stable states. It is capable to function as a memory.

A flip-flop is controlled by one or two control signals and/or a gate or clock signal. The output often includes the complement as well as the normal output.

Sometimes they have separate auxiliary clear and load/set/preset inputs too.

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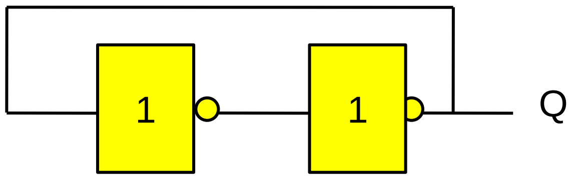
FLIP-FLOPS: ELECTRONICS

The basis for the flip-flops is an amplifier with a positive feedback (pair of simple transistor amplifying stages, or one amplifying stage and a transformer for creating the positive feedback, etc.).



In digital technique a pair of inverters or logical elements with similar behaviour are often used.
This circuit can have two stable states, either Q = 0 or Q = 1

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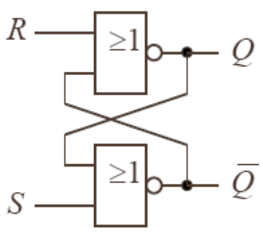
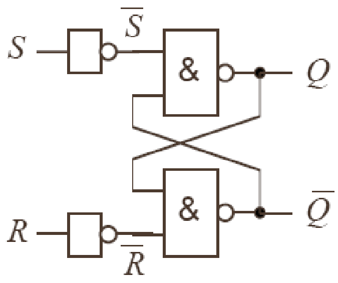
BASIC SET/RESET CIRCUIT (BISTABLE)



S	R	Q	$\overline{Q}$
0	0	Q_{-1}	$\overline{Q}_{-1}$
0	1	0	1
1	0	1	0
1	1	(0)	(0)

Q is on the R "side" !

NOR gate: 1 on any input forces the output to 0!



S	R	Q	$\overline{Q}$
0	0	Q_{-1}	$\overline{Q}_{-1}$
0	1	0	1
1	0	1	0
1	1	(1)	(1)

Q is on the S "side" !

NAND gate: 0 on any input forces the output to 1!

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FLIP-FLOPS

The most important flip-flops are the following:

R-S (or S-R) flip-flop	set/reset
J-K flip-flop	set/reset/toggle
T flip-flop	toggle
D flip-flop	data/delay
D-G flip-flop	

All flip-flops listed above can function in synchronous or clocked mode, the R-S and D flip-flops can operate in asynchronous mode too.
The behaviour of a particular type can be described by truth/characteristic table and the characteristic equation, which gives the next output in terms of the input control signals and the current output.

OPERATION OF FLIP-FLOPS

-The change of state of asynchronous flip-flops occurs directly as a response to the change of the input/control variable(s), after the appropriate time delay of the circuit.

-The change of state of synchronous (clock controlled) flip-flops occurs only when the synchronizing signal (clock) arrives tot heir appropriate input.

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FLIP-FLOPS: STATIC AND DYNAMIC CONTROL

The control of flip-flops can be

either static or dynamic.

Static: appropriate logic 0 and/or 1 levels should be applied to the static control inputs to initiate the state changes.

Dynamic: the change of state of the flip-flop occurs due the change in the appropriate direction (1→0 or 0→1 transition) of the signal applied to the dynamic control input (edge-triggered).

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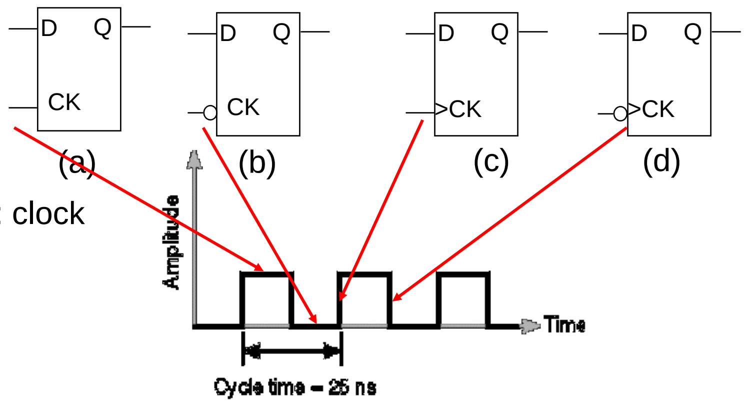
FLIP-FLOPS: NOTATIONS



CK: clock

(a) **CK=1**, (b) **CK=0** levels activate the information transfer

(c) **CK** rising edge, (d) **CK** falling edge activates the FF.

Usualy **S** (set, **PR** preset), **R** (reset,**CLR** clear) inputs and **Q#** output is also provided.

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RS FLIP-FLOP: INTRODUCTION

The SR (set/reset) flip-flop is the simplest flip/flop used in digital systems. It can be realized/implemented by direct feedback of a combinational circuit, i.e. with asynchronous sequential circuit.

Some features:

- Two control inputs: Reset and Set
- Two (complementary) outputs
- Three allowed (defined)and one forbidden (undefined) outputs
- The allowed states are stable
- The forbidden state can be unstable

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RESET-SET (R-S) FLIP-FLOP (1)

SET loading, RESET clearing, independently of the pervious state.

”Simple” truth table

R	S	Q^{n+1}
0	0	Q^n
0	1	1
1	0	0
1	1	X

Defined operation:
S = 1 sets the FF state to 1, and it holds this state even after the termination of control.
R = 1 stes the FF state to 0, and it holds this state even after the termination of control.
If S and R are simultaneously 0 the state of the FF does not change, it holds its previous state.
If S and R are simultaneously 1 , the FF functioning is not defined, therefore this control combnination is logically forbidden.

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RS FLIP-FLOP: CASE OF R=S=1

For the R=S=1 input combination the output is not defined, so this input combination is not allowed.

However a given circuit implementation will produce a certain, mostly well define output state for this input.
E.g. The NOR gate based circuit will give 0 logic level on both (direct and complementary) output, the NAND based circuit will give logic level 1 on both output.
In these cases the complementary relation between the two outputs is not fulfilled.
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RS FLIP-FLOP: ”MEMORY”

From the truth table, we can develop a sequence such as the following:

1. R = 0, S = 1 $\Rightarrow$ Q = 1 (set)
2. R = 0, S = 0 $\Rightarrow$ Q = 1 (Q = 1 state retained: ”memory")
3. R = 1, S = 0 $\Rightarrow$ Q = 0 (reset)
4. R = 0, S = 0 $\Rightarrow$ Q = 0 (Q = 0 state retained)

In alternative language, the first operation ”writes" a true state into one bit of memory.
It can subsequently be ”read" until it is erased by the reset operation of the third line.

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R-S FLIP-FLOP (2)

Extended truth table

n-th		(n+1)-th state		
R	S	Q^n	Q^{n+1}	
0	0	0	0	does not change
0	0	1	1	does not change
0	1	0	1	toggles
0	1	1	1	does not change
1	0	0	0	does not change
1	0	1	0	toggles
1	1	0	X	undefined
1	1	1	X	undefined

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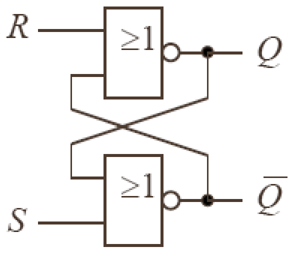
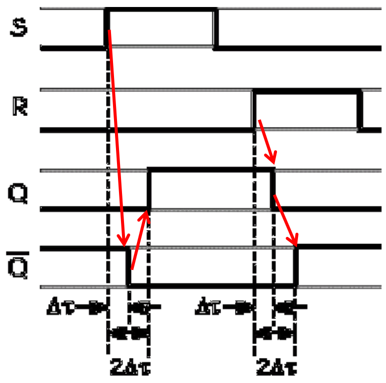
S-R (SET-RESET) FLIP-FLOP: TIMING BEHAVIOUR





The S-R flip-flop implemented with NOR gates is an active high (positive logic) device.

INVERSE R-S FLIP-FLOP

$\overline{R}$	$\overline{S}$	Q^{n+1}
0	0	X
0	1	0
1	0	1
1	1	Q^n

The inverse RS flip-flop is controlled by the 0 levels.

Implementation: two cross coupled NAND gates.

For the logically undefined input combination both NAND gates give 1 on their outputs.

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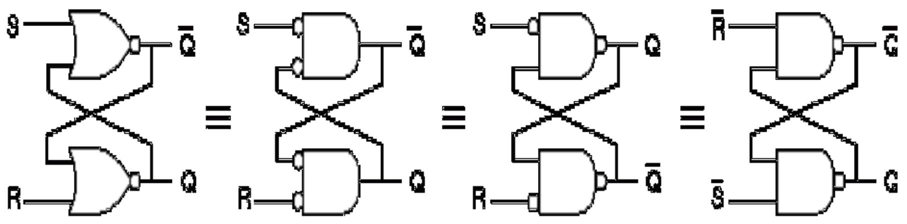
NOR S-R ↔ NAND S-R CONVERSION



Active High NOR Implementation.

Push Bubbles (DeMorgan's)

Rearrange Bubbles

Convert from Bubbles to Active Low Signal Names

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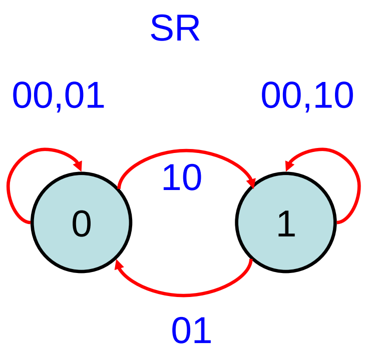
R-S FLIP-FLOP: STATE TABLE AND TRANSITION DIAGRAM

Q^{n+1}

Q^n \ SR	00	01	11	10
0	0	0	X	1
1	1	0	X	1



No oscillation can develop in any of the column, the operation can be defined both in asynchronous and synchronous mode. (Red: stable states.)

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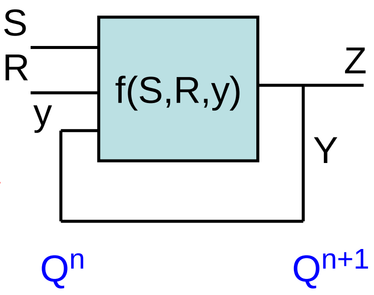
ASYNCHRONOUS R-S FF (LATCH): IMPLEMENTATION WITH COMBINATIONAL NETWORK

The state transition table can be considered as a Karnaugh table

$Q^{n+1} = S + \overline{R}\, Q^n$

			S	S
	0	0	X	1
Q^n	1	0	X	1
		R	R	



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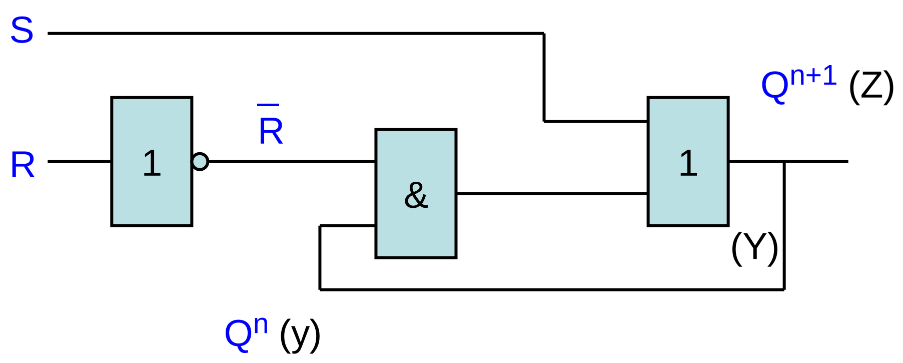
AND-OR GATE IMPLEMENTATION: LOGIC DIAGRAM

$Q^{n+1} = S + R\,\overline{Q}^n$ characteristic equation implemented:



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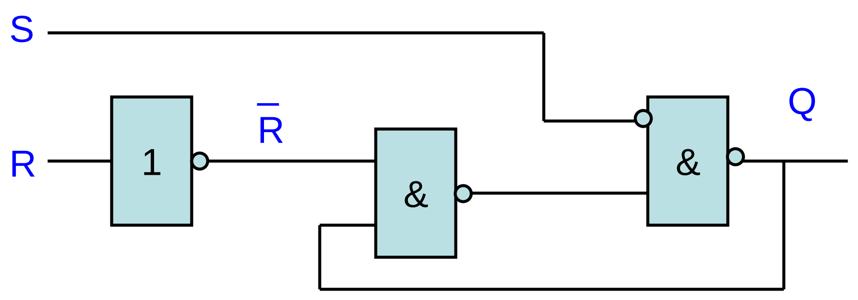
TRANSFORMATION TO NAND-NAND REALIZATION

Transformation according DeMorgan's law



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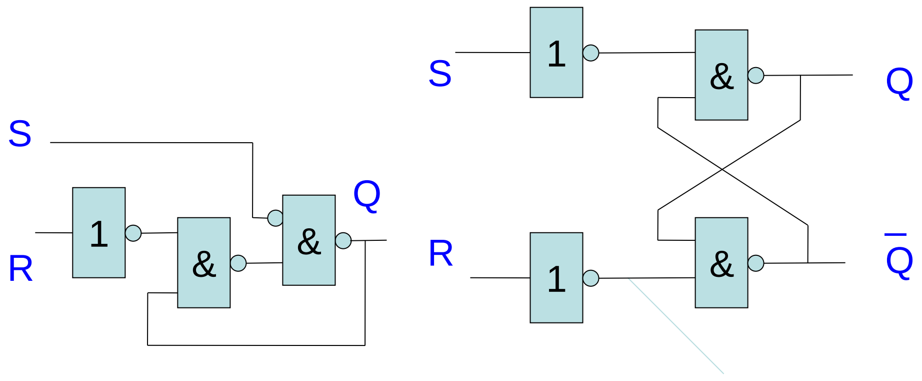
TRANSFORMATION TO NAND-NAND REALIZATION

Transformation according DeMorgan's law and rearranging/redrawing the circuit:



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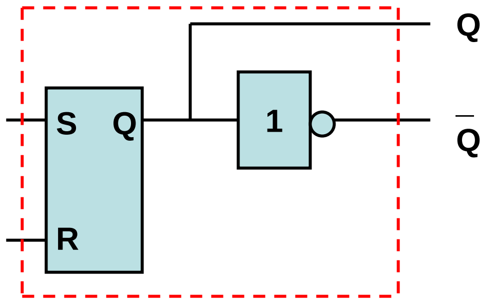
SR FLIP-FLOP

The problem of logically undefined state (S = R =1) can be handled by using an additional inverter to generate Q` from Q (for NAND gate realization):



For the excitation SR =1 the output will be Q = 1, i.e. the S input has the priority.

RS FLIP-FLOP: ENHANCEMENTS

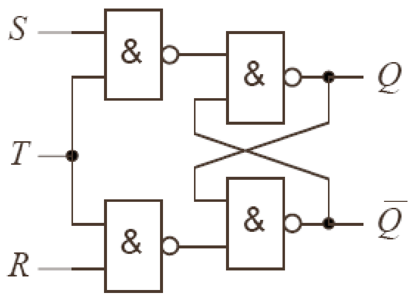
Solution:

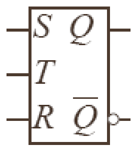
State change initiated by clock: gated RS flip-flop

JK flip-flop

D flip-flop

GATED/CLOCK-CONTROLLED RS FLIP-FLOP





The gate input can also accept a CLOCk signal: synchronous operation

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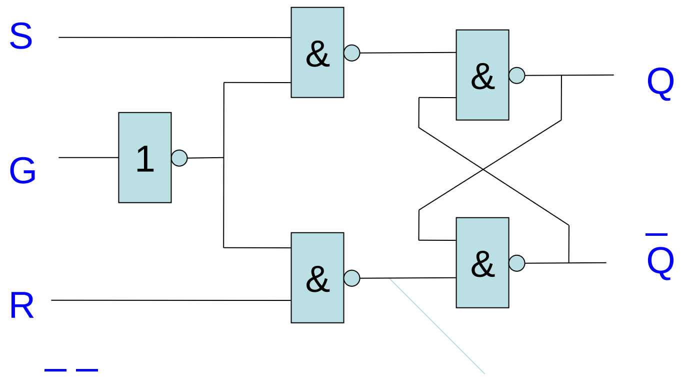
GATED RS FLIP-FLOP

State change : 0→1 transition on G



$Q^{n+1} = SG + \overline{R}\overline{G}\, Q^n$

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R-S FLIP-FLOP: EMPHASIS

- The RS flip-flop is typically an asynchronous circuit.

- RS flip-flops are nor produced/used for/in networks, because other flip-flop types are more effective (they don't have forbidden states).

- However synchronous flip-flops usually contain asynchronous, static zeroing (RESET) and loading (SET ior PRESET) facilities.

- The RS flip-flop is the basic unit of semiconductor memories (SRAM, static random access memory).

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JK FLIP-FLOP (1)

The JK flip-flop augments the behaviour of the SR flip-flop by interpreting the S = R = 1 conditions as a "flip" ("toggle") command:

J	K	Q_{next}	Comment
0	0	Q_{prev}	hold state
0	1	0	reset
1	0	1	set
1	1	$\overline{Q}_{prev}$	toggle

SR-JK correspondence:

$$S \Rightarrow J$$

$$R \Rightarrow K$$

In a certain respect it is an enhanced version of the RS FF. Logic/control function is defined to the originally not-allowed control combination of the RS FF.

J-K FLIP-FLOP (32

"Simple" truth table

J	K	Q^{n+1}
0	0	Q^n
0	1	0
1	0	1
1	1	$\overline{Q}^n$

Defined functioning:

J = 1 K = 0 sets FF state to 1,
K = 1 J = 0 sets FF state to 0,
If J and K is simultaneously 0 the state does not change.

If J and K is simultaneously 1 the state of the FF is complemented.

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J-K FLIP-FLOP (4)

Extended thuth table

n-th		(n+1)-th state		
J	K	Q^n	Q^{n+1}	
0	0	0	0	holding state
0	0	1	1	holding state
0	1	0	0	zeroing (set 0)
0	1	1	0	zeroing (set 0)
1	0	0	1	setting (set 1)
1	0	1	1	setting (set 1)
1	1	0	0	complementing
1	1	1	1	complementing

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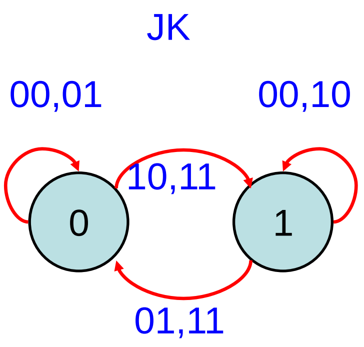
J-K FLIP-FLOP: STATE TABLE AND GRAPH

Q^n \ JK (Q^{n+1})	00	01	11	10
0	0	0	1	1
1	1	0	0	1



No stable state exist in the J=K= 1 column. The JK FF can only be operated as a synchronous circuit. Cannot operate without gating/clocking signal.

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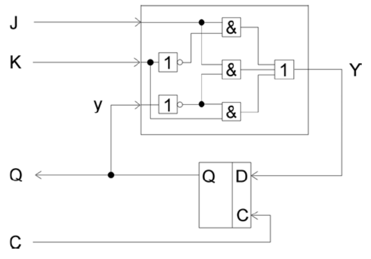
J-K FLIP-FLOP: CHARACTERISTC EQUATION

Implementation „in principle”

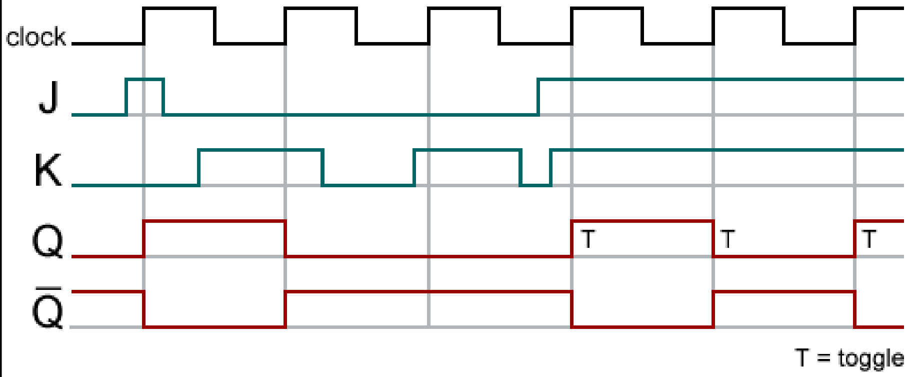


			J	J
	0	0	1	1
Q^n	1	0	0	1
		K	K	

The third term in the equation is necessary for the elimination of race hazards

$$Q^{n+1} = J\,\overline{Q}^n + \overline{K}\,Q^n + J\,\overline{K}$$

J-K FLIP-FLOP: TIME DIAGRAM



J	1	0	0	1	1	1
K	0	1	1	1	1	1

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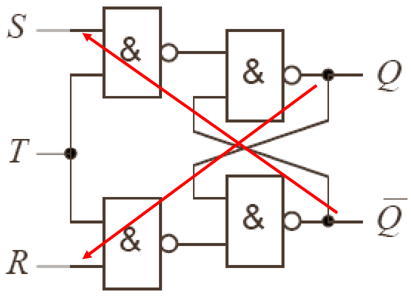
JK FF BUILT ON THE BASIS OF RS FF

The JK flip-flop can be built fro gated RS FF of the R input is gated with the Q output, and the S input is gated with the /Q output.



The indicated gating/feedback ensures the R = S = 1 input state would not occur!

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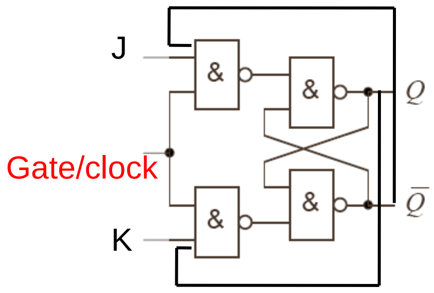
GATED/CLOCKED JK FF OPERATION

The operation of JK FF can be demonstrated by its characteristic equation.
The ”original” RS flip-flop

$$Q^{n+1} = S + \overline{R}\, Q^n$$



Applying the feedback

$S = J\,\overline{Q}^n$ and $R = K\,Q^n$

$$Q^{n+1} = S + \overline{R}\, Q^n = J\,\overline{Q}^n + (\overline{K} + \overline{Q}^n)\, Q^n =$$

$$J\,\overline{Q}^n + \overline{K}\, Q^n$$

Q. E. D.

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GATED JK FLIP FLOP

Similarly as in the case of gated RS FF in the case of gated JK FF the control signals exert their influence only when the gate signal is 1.

If the width of the gating pulse on input G is less than the signal propagation time through the two gates, then for J = K = 1 the FF will change its state only once in response to the gate signal.

On the other hand a too short gate signal width can result in an uncertain operation, because the too short signals might not push the FF int the correct state.

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MASTER-SLAVE FLIP-FLOP

The JK flip-flops used in practice mostly operate on the basis of master-slave principle. The master-slave flip-flops consist of two elementary storage cells, the first is the master, the second is the slave.

The principle of operation, and its realization will be demonstrated on the example of RS flip-flop.

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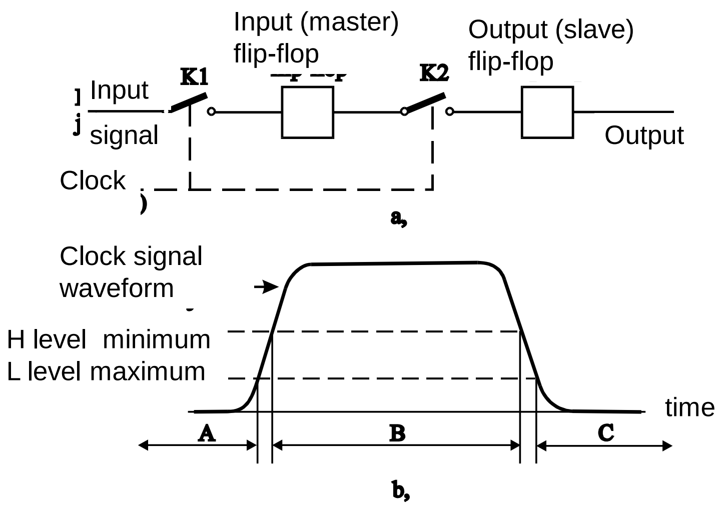
TWO-CYCLE (MASTER-SLAVE) STORAGE CELL (FLIP-FLOP) PRINCIPLE

The two switches operate in opposite cycle!



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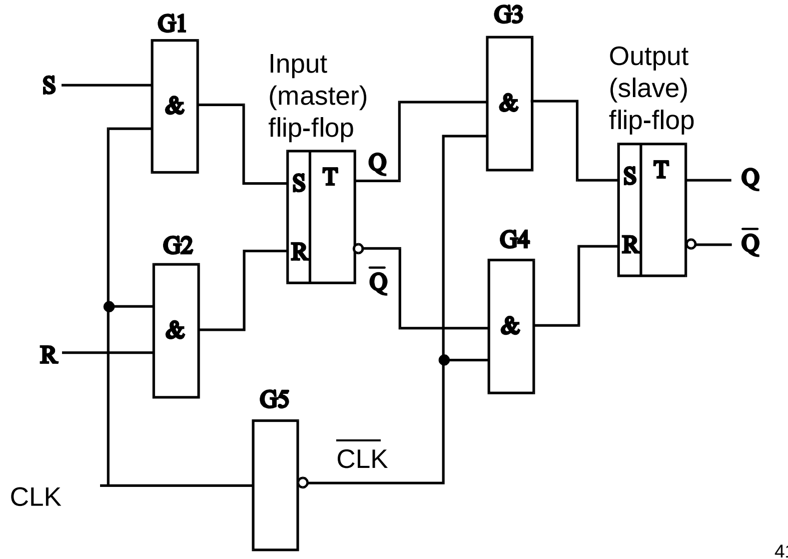
TWO-CYCLE (MASTER-SLAVE) RS FF



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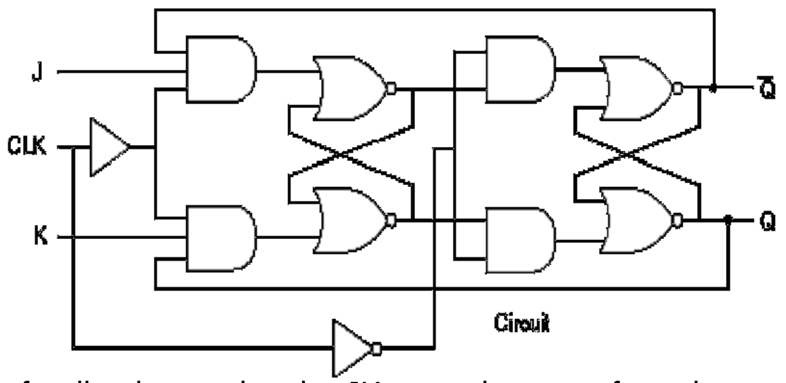
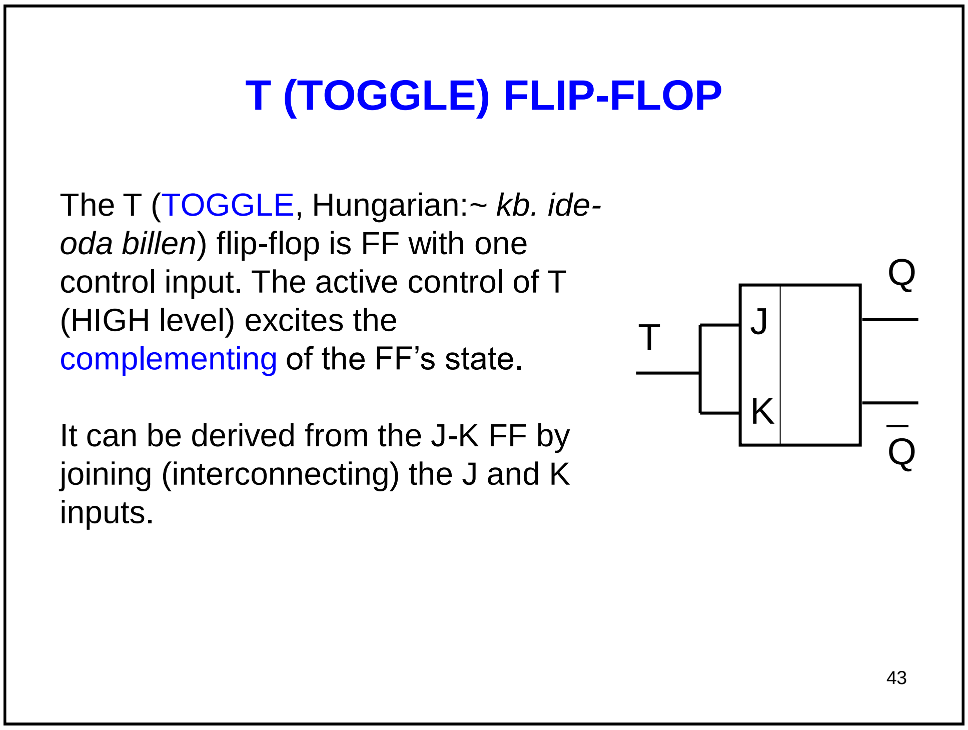
THE MASTER-SLAVE JK FLIP-FLOP



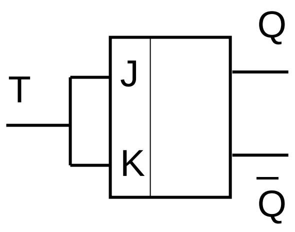
The feedback ensuring the JK operation goes form the outputs of the slave FF to the control inputs of the master FF!



T (TOGGLE) FLIP-FLOP

The T (TOGGLE, Hungarian:~ *kb. ide-oda billen*) flip-flop is FF with one control input. The active control of T (HIGH level) excites the complementing of the FF's state.

It can be derived from the J-K FF by joining (interconnecting) the J and K inputs.



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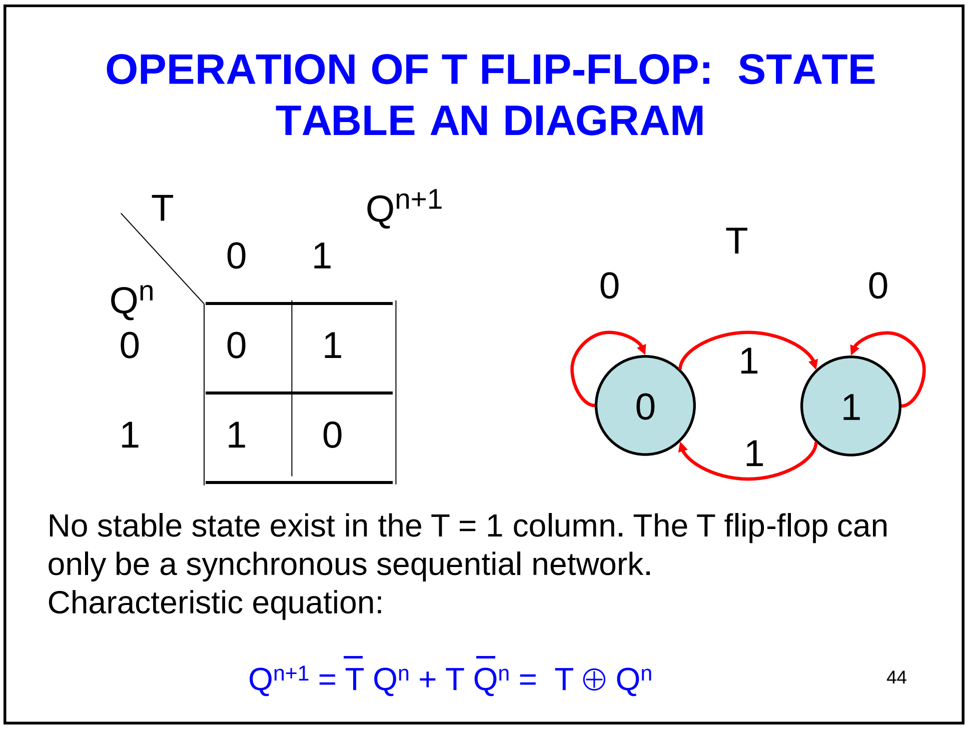
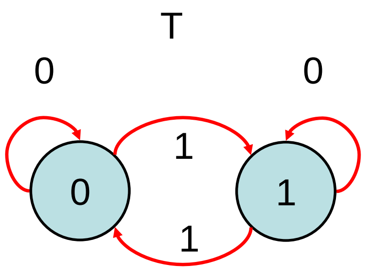


OPERATION OF T FLIP-FLOP: STATE TABLE AN DIAGRAM

$$\begin{array}{c|cc}
Q^n \backslash T & 0 & 1 \\
\hline
0 & 0 & 1 \\
1 & 1 & 0
\end{array} \quad Q^{n+1}$$



No stable state exist in the T = 1 column. The T flip-flop can only be a synchronous sequential network.
Characteristic equation:

$$Q^{n+1} = \overline{T}\,Q^n + T\,\overline{Q^n} = T \oplus Q^n$$

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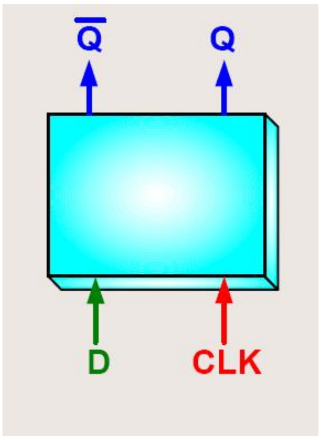
T FLIP-PLOP

T flip-flops do not really exist, constructed from JK or D FFs.

Usually best choice for implementing counters.

To create a T-FF using a D: Add a feedback connection that makes the input signal D equal either the value of Q or Q' under the control of the signal T.

D FLIP-FLOP (1)



The state of the Q output of the D (DELAY) flip-flop Q in the next, (n+1)-th state will be equal to the state of the D control input in the pevious, n-th state:

$$Q^{n+1} = D^{n}$$

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D FLIP-FLOP (2)

Truth table and characteristic equation

n-th		(n+1)-th state
D	Q^n	Q^{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$Q^{n+1} = D$

In fact the state in the (n+1)-th state in fac t will nt depend on what was the state of the FF in the n-th state!
The D flip-flop does not remember its previous stater

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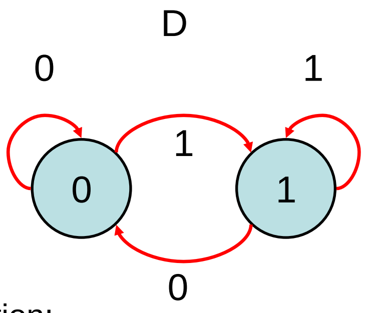
D FLIP-FLOP: STATE TABLE AND STATE TRANSITION DIAGRAM

Q^{n+1}

Q^n \ D	0	1
0	0	1
1	0	1



Characteristic equation:

$Q^{n+1} = D$

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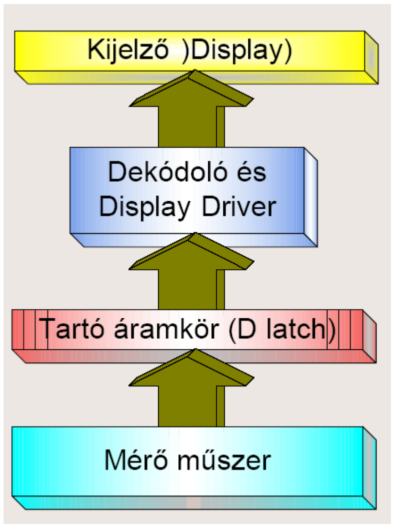
A D FLIP-FLOP (3)



-The D flip-flop is mostly used to as a component in storage registers.

-E.g.to store the value displayed by a digital instruments, till the value of the new reading arrives.

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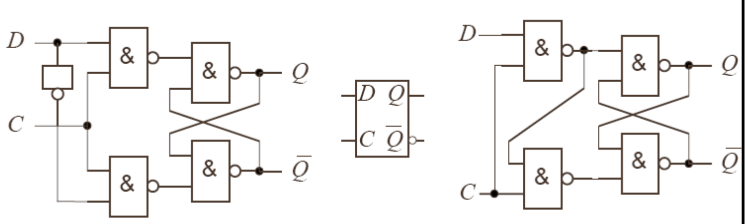
D FLIP-FLOP WITH CLOCK

C	D	Q	$\overline{Q}$
0	0	Q_{-1}	$\overline{Q}_{-1}$
0	1	Q_{-1}	$\overline{Q}_{-1}$
1	0	0	1
1	1	1	0



Operation of D (DELAY) flip-flop with synchronizing clock. If there is no clock signal (C=0) the output does not change ($Q^n = Q^{n-1}$), if there is a clock signal (C=1) the output will take the actual value of the input, i.e. Q^n = D.

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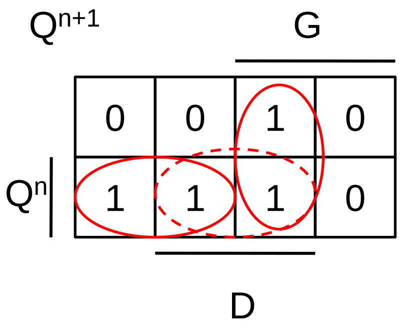
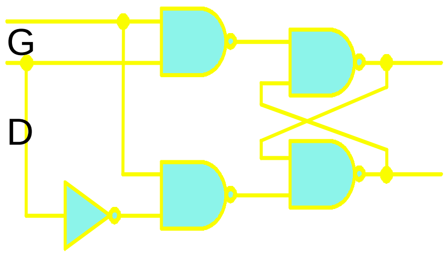
GATED D FLIP-FLOP



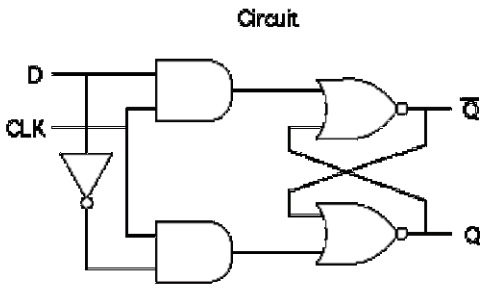


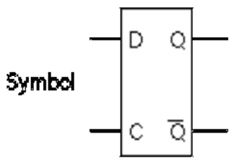
$Q^{n+1} = D\,G + \overline{G}\,Q^n + D\,Q^n$

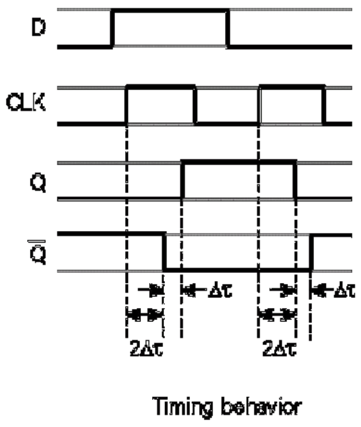
3rd loop: hazard elimination

Operation can be asynchronous or synchronous.

TIME DIAGRAM OF GATED D FLIP-FLOP







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CHARACTERISTIC EQUATIONS OF FLIP-FLOPS: A SUMMARY

RS	$Q^{n+1} = S + \overline{R}\, Q^n$
JK	$Q^{n+1} = J\, \overline{Q}^n + \overline{K}\, Q^n + J\, \overline{K}$
T	$Q^{n+1} = \overline{T}\, Q^n + T\, \overline{Q}^n = T \oplus Q^n$
D	$Q^{n+1} = D^n$
D-G	$Q^{n+1} = D\, G + \overline{G}\, Q^n + D\, Q^n$

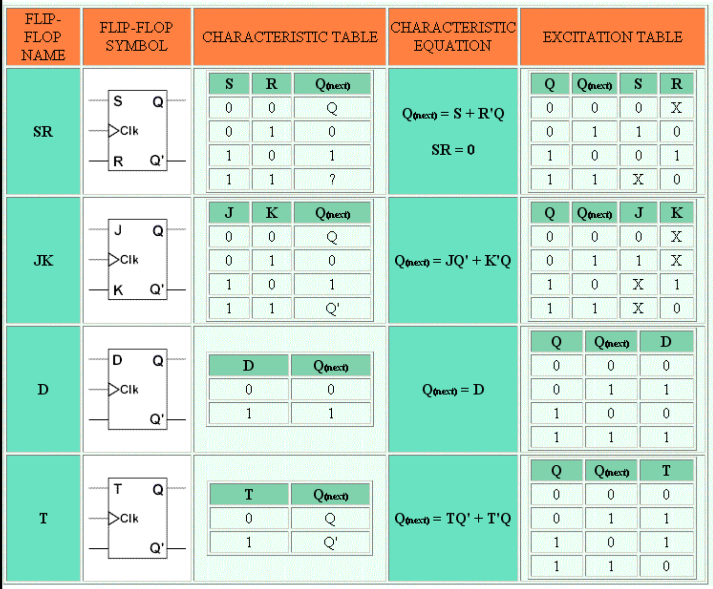
Note: The third terms in the equation of JK and D-G flip-flops serve for the elimination of race hazards

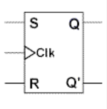
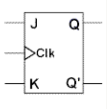
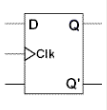
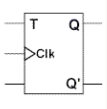
EXCITATION TABLES OF FLIP-FLOPS

Q^n	Q^{n+1}	R	S	J	K	D	T
0	0	x	0	0	X	0	0
0	1	0	1	1	X	1	1
1	0	1	0	X	1	0	1
1	1	0	X	X	0	1	0

The excitation table lists the required inputs for a given change of state, i.e. the input conditions that will cause the transition form a given present state to the next state.
The excitation table is required and is used in the design process.

SUMMARY OF FLIP-FLOP TYPES



FLIP-FLOP NAME	FLIP-FLOP SYMBOL	CHARACTERISTIC TABLE	CHARACTERISTIC EQUATION	EXCITATION TABLE
SR		S R $Q_{(next)}$ 0 0 Q 0 1 0 1 0 1 1 1 ?	$Q_{(next)} = S + R'Q$ $SR = 0$	Q $Q_{(next)}$ S R 0 0 0 X 0 1 1 0 1 0 0 1 1 1 X 0
JK		J K $Q_{(next)}$ 0 0 Q 0 1 0 1 0 1 1 1 Q'	$Q_{(next)} = JQ' + K'Q$	Q $Q_{(next)}$ J K 0 0 0 X 0 1 1 X 1 0 X 1 1 1 X 0
D		D $Q_{(next)}$ 0 0 1 1	$Q_{(next)} = D$	Q $Q_{(next)}$ D 0 0 0 0 1 1 1 0 0 1 1 1
T		T $Q_{(next)}$ 0 Q 1 Q'	$Q_{(next)} = TQ' + T'Q$	Q $Q_{(next)}$ T 0 0 0 0 1 1 1 0 1 1 1 0

S=R=1 not allowed

Most versatile type

Most simple Gated (DG) Copies input to output

Complements output if activated

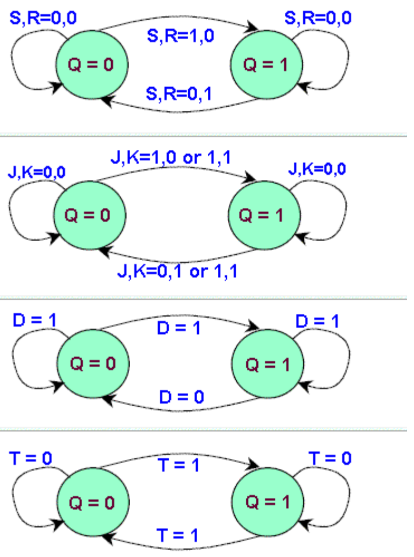
STATE TRANSITION DIAGRAMS: SUMMARY

SR flip-flop

JK flip-flop

D flip-flop

T flip-flop



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REVISION QUESTIONS

1. What is the difference in the operation of edge-triggered FFs and master slave FFs?

2. Justify name Toogle for T flip-flop giving truth table and waveforms.

3. Give the characteristic equation for each flip-flop.

4. Draw the state transition diagrams for SR, D, JK and T flip-flop.

5. Derive the excitation tables for SR, D, JK and T flip-flop.

REVISION QUESTIONS

6. Explain the major difference between RS and JK flip-flops.

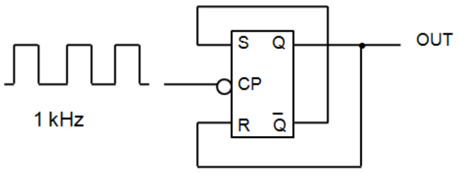
7. Show the logic diagram of a clocked D fl ip-fl op with four NAND gates.

8. Draw the logic diagram of master-slave D fl ip-fl op. Use NAND gates.

PROBLEMS AND EXERCISES

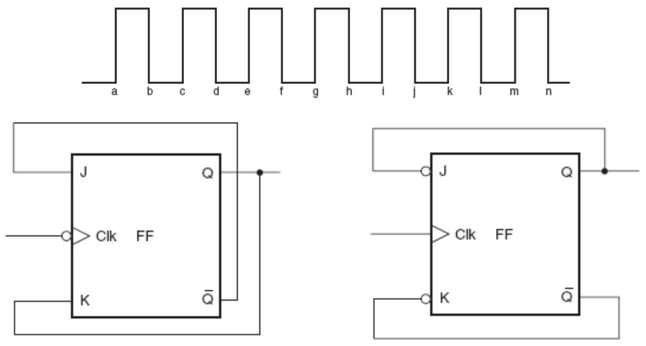
1. Analyze the operation of the type 7474 edge triggered D flip-flop and give its full operational/truth table for asynchronous and synchronous control.

2. Consider the-self gated flip-flop below and determine and draw its output waveform with respect the input signal.



PROBLEMS AND EXERCISES

3. The 100 kHz square waveform shown below is applied to the clock input of the flip-flops shown in the figures. If the Q output is initially ‘0’, draw the Q output waveform in the two cases. Also, determine the frequency of the Q output in the two cases.


a b c d e f g h i j k l m n
J
Q
Clk
FF
K
Q̄