DIGITAL TECHNICS II

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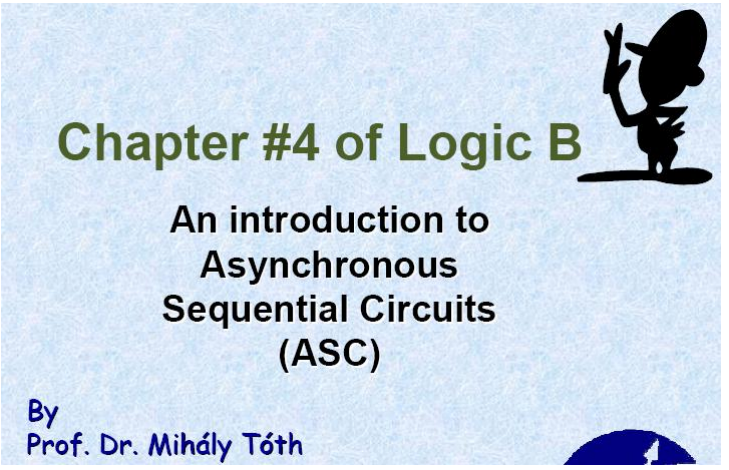
ASYNCHRONOUS SEQUENTIAL CIRCUITS: AN INTRODUCTION

2nd (Spring) term 2017/2018

INTRODUCTION



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THE FUNDAMENTAL MODE OF OPERATION (FMO)

- FMO is a very common operating principle of every logic circuit.
- Its essence is to separate the external and internal transients
- That is during the internal transients of a circuit its inputs must be steady,
  (otherwise we cannot predict the next state of that circuit.)
- The FMO condition must be guaranteed for every kind of logic circuits.

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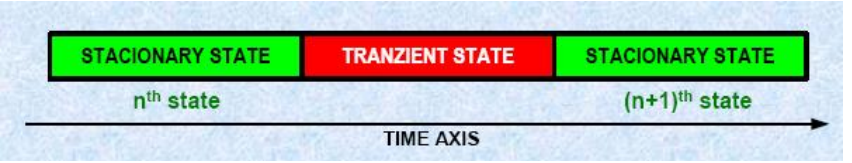
STATIC MODEL OF SEQUENTIAL CIRCUITS



The static model describes the so called event history of the circuits, but not its transients.

In the state functions the time as variable does not occur.

This model can also be applied in the case of asynchronous sequential circuits as well.

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HOW TO ENSURE THE FMO CONDITION?

In case of combinational circuits after any change of the input state we have to wait until the propagation delay of the actual circuit is over, then read the output state.
(Think of an address-change of a ROM.)

In case of synchronous sequential circuits the clock period must be equal or longer then the longest transient which may occur in the given circuit.

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HOW TO ENSURE THE FMO CONDITION IN AN ASC?

Really this is the fundamental problem in asynchronous sequential circuits (ASCs).
We have to apply some tricks in case of every ASC.

The advantage to be gained is a faster operation than in the casa of a SSC.

In some cases this question cannot be suppressed. E.g. if we want to analyze or synthesize the internal circuitry of a flip-flop (which may seem to be a synchronous one looking from the outside of the flip-flop itself).

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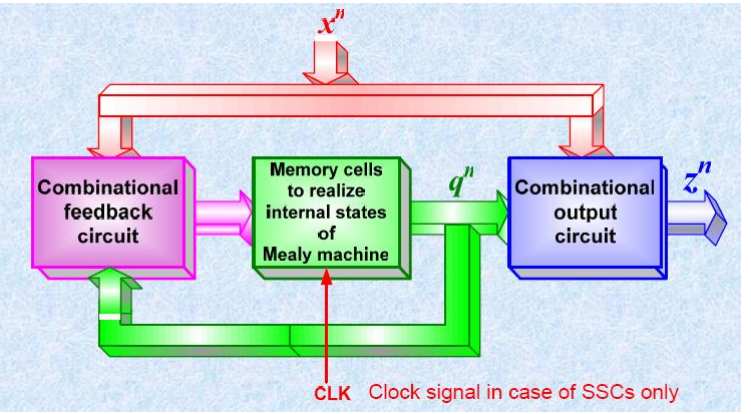
LOGIC STRUCTURE OF THE MEALY MACHINE



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TRIGGERING AN ITERNAL TRANSITION

In the case of an SSC there exists a special input, that is the clock, to guarantee that during the internal transients any (preparatory) input has no effect on the operation.

In the case of ASCs there is no such special input.

Any input-change of the circuit may cause a state-change, i.e. an internal transition.

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REAL SEQUENTIAL CIRCUITS

Q: Is there any „pure” SSC?

A1: Practically not. If we look „deep” enough to an SC (into its flip-flops inside) then the only model we can apply is the ASC model.

A2: In case of a large circuit in which the operating speeds of the different components may exhibit great differences, the communication among the components could only be asynchronous.

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MORE ON REAL SEQUENTIAL CIRCUITS

If we look inside the flip-flops that means

We do not identify the flip-flops as special components of an SC. (We identify loops instead.)

Naturally we do not find (some smaller) flip-flops within the flip-flops. (It’s not like the case of atomic and elementary particles.)

In can be shown that the memory as such is inseparable from the feedback.

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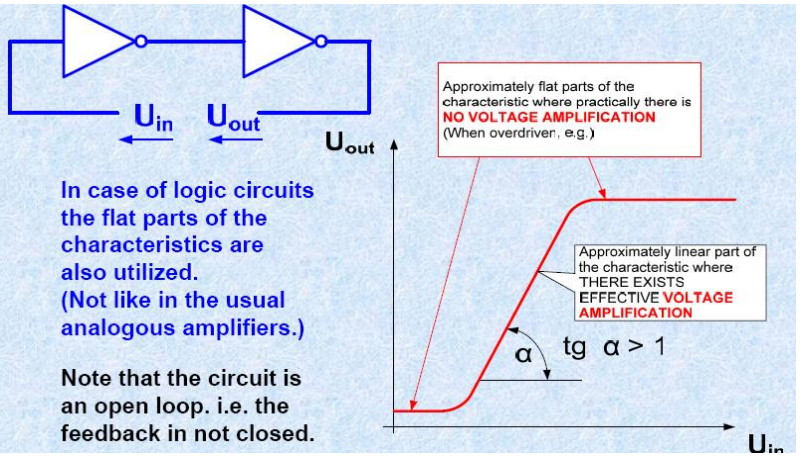
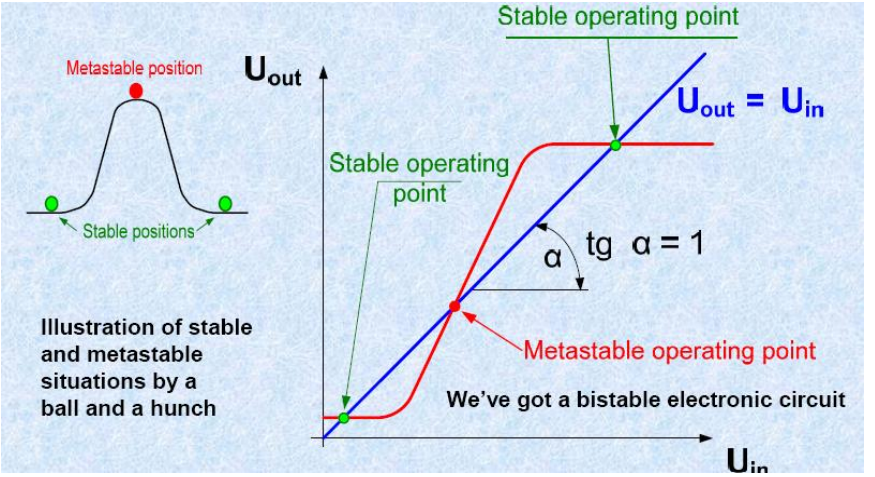
LOGIC CIRCUIT WITH FEEDBACK: TWO STAGE AMPLIFIER



Analysis of the properties of a two-stage feedback amplifier feedback loop open

TWO STAGE AMPLIFIER WITH CLOSED FEEDBACK LOOP



The result is a bistable electronic ciircuit.

CONTROLLING THE STATE-CHANGE

Instead of simple inverters two-input gates having voltage amplification are used.

Such appropriate logic gates are the NOR and NAND gates.

Both of them are suitable for constructing the static (asynchronous) flip-flop.

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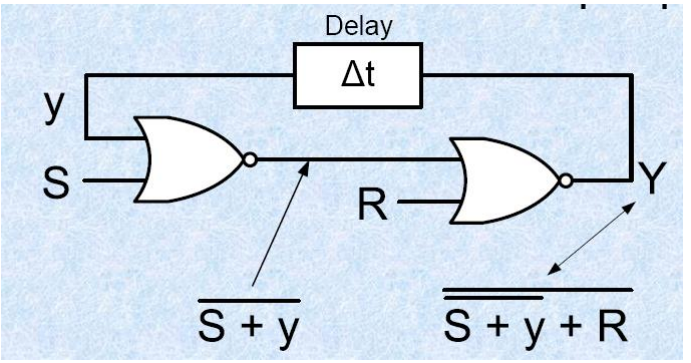
THE DOUBLE NOR STATIC FLIP-FLOP



The double NOR static flip-flop

The two NOR gates are idealized and their always existing propagation delays are concentrated here to Δt.
Note the closed feedback loop.

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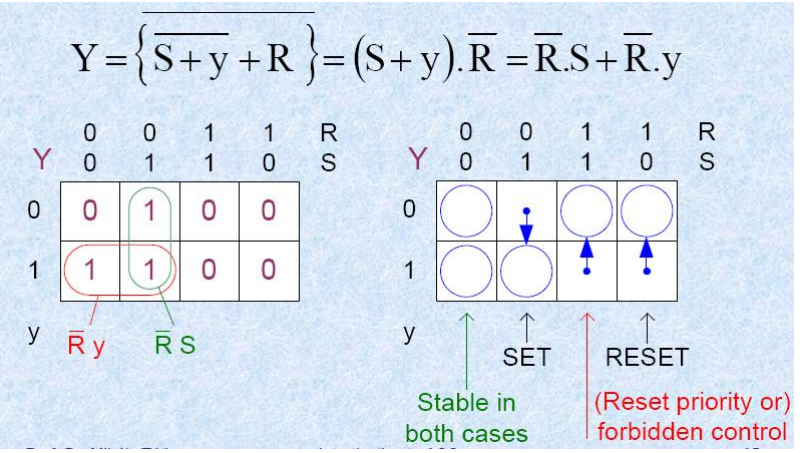
THE CONTROL FUNCTION

$$Y = \left\{ \overline{\overline{S + y} + R} \right\} = (S + y).\overline{R} = \overline{R}.S + \overline{R}.y$$



The so called control function (Y) of the circuit having a feedback.

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THE CONDITION FO A STABLE STATE

Theoretically Y is determined in the same time instant when the inputs are asserted.

After passing the appropriate Δt time, the logic value of Y will be the same as y was before.

If y = Y, then there will be no change in the inputs, i.e. the circuit is in stable state.

Consequently the condition of a state being stable is y = Y.

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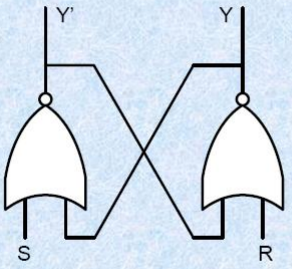
STATIC (ASYNCHRONOUS) FLIP-FLOP

The usual circuit diagram of a **static** (asynchronous) **RS flipflop**

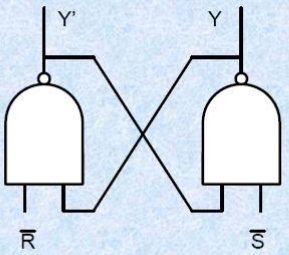


- The Set and Reset control inputs
  - are activated by High logic level
  - should not be activated simultaneously

Y' is the negated value of **Y** only iff the control combination of **R = S = 1 is never asserted** to the inputs. This is why it's a forbidden input control combination.

THE DOUBLE NAND STATIC FLIP-FLOP

The **double NAND** static flipflop



- The Set and Reset control inputs
  - are activated by Low logic level
  - should not be activated simultaneously

Y' is the negated value of **Y** only iff the control combination of **$\overline{R}$ = $\overline{S}$ = 0 is never asserted** to the inputs. This is why it's a forbidden input control combination.
Note the closed loop which realizes 1 bit memory.

END

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