DIGITAL TECHNICS II

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4. LECTURE: REGISTERS AND RELATED

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4. LECTURE: REGISTERS

1. Storage registers
2. Shift registers
3. Register application examples
4. Register counters

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REGISTERS: AN INTRODUCTION

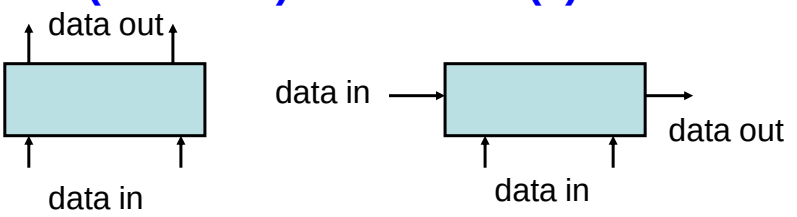
Registers are devices which are used to store and/or shift data entered from external sources. They are constructed by connecting a number of flip-flops in cascade.

A single flip-flop can store 1 bit of data, thus an n-bit register will require n flip-flops.

In a digital system such registers are generally used for temporary storage of data.

Registers can hold data supposed the supply voltage is continuous.

LOADING (INPUT) AND READING (OUTPUT) METHODS (1)



parallel loading and reading

series/parallel input series output

In case of series input and/or series output the data are transferred from one position to the next one, therefore there circuit connections between the neighbouring positions.

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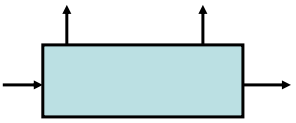
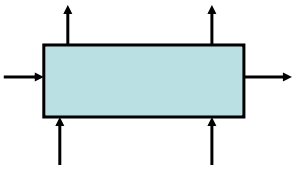
LOADING (INPUT) AND READING (OUTPUT) METHODS (2)



Series input, parallel or series output

series input and output



series/parallel input/output

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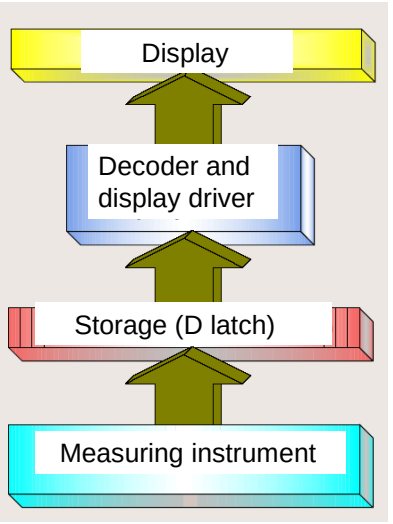
REGISTERS: PROPERTIES AND CLASSIFICATION

Classification according to internal structure and operation/function:

- storage register;
- shift register

Storage register: it takes data from parallel inputs and copies it to the corresponding output when the registers are clocked. It can be used as a kind of “history”, retaining old information as the input in another part of the system, until ready for new information, whereupon, the registers are clocked, and the new data is “let through”. It is usually built using D flip-flops.

D FLIP-FLOP & REGISTER



-The D flip-flop is mostly used to as a component in storage registers.

-E.g.to store the value displayed by a digital instruments, till the value of the new reading arrives.

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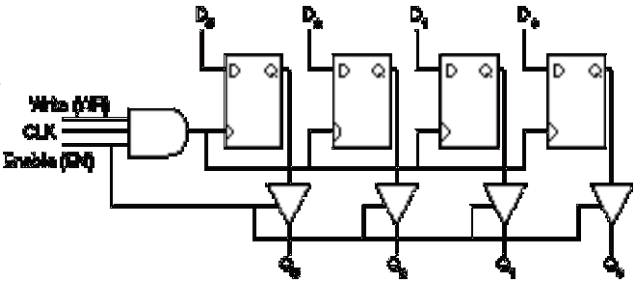
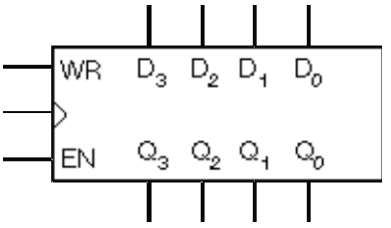
STORAGE REGISTERS

Gate level view



Chip level view



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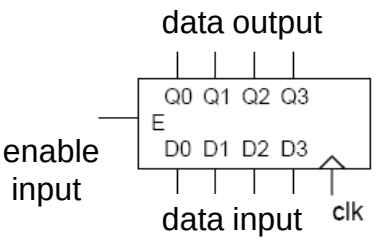
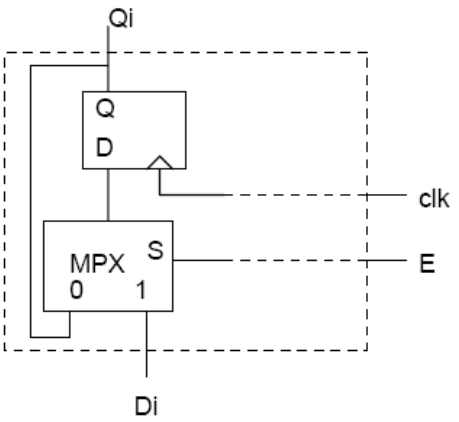
STORAGE REGISTER WITH ENABLE

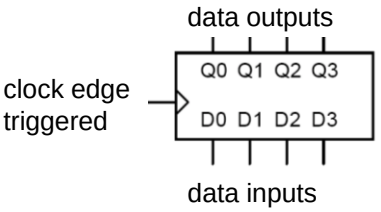




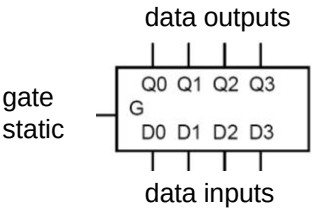
E = 0 hold
E = 1 write

REGISTER, LATCH

A registers are composed of D or DG flip-flops usually having common clock/gate and clear inputs (MSI IC: 4- or 8-bit). D flip-flop: register, DG flip-flop: latch.



Register
(common clock)



Latch
(common G input)

USES OF STORAGE REGISTERS

- arithmetical units;
- temporary storage between counter and display;
- code and signal conversion operations;
- input/output storage registers in µPs;
- intermediate storage functions in arithmetic/logic units (ALU);
- various types of other temporary storage functions.

SHIFT REGISTERS

- The shift function of a register allows the stored data to be moved serially from stage to stage or into or out if the register.

- Types of data movement:
  - serial shift right or left
  - parallel shift in to and out

- The shift is executed by the synchronizing or clock signal.

- Register are used for conversion of data form serial to parallel and vice versa. Also used as counters.

- In shift registers the flip-flop types used should not be transparent. Usually master-slave types are used.

SHIFT REGISTERS: CHARACTERISTIC EQUATIONS

Right shift register:

$$Q_i^n = Q_{i+1}^{n-1}$$

Left shift register:

$$Q_i^n = Q_{i-1}^{n-1}$$

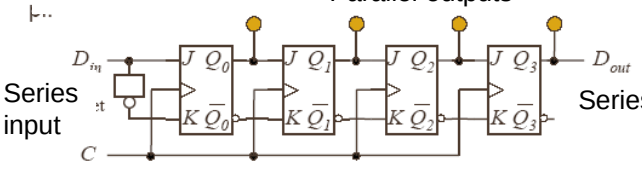
Bi-directional shift register
Right sift (M=1) - left shift (M = 0):

$$Q_i^n = \overline{M}\, Q_{i-1}^{n-1} + M\, Q_{i+1}^{n-1}$$

SHIFT REGISTER

In a shift register the information stored in the FFs shift to right or left for each clock pulse. Can be used to series-to-parallel or to parallel-to series conversion.

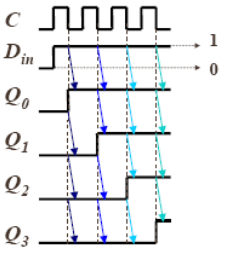
Parallel outputs



Series input

Series output

E.g. if input is constantly 1, the register will be filled with four 1s after the fourth step.



lépés	Q_3	Q_2	Q_1	Q_0
-	0	0	0	0
1.	0	0	0	D_1
2.	0	0	D_1	D_2
3.	0	D_1	D_2	D_3
4.	D_1	D_2	D_3	D_4

SHIFT REGISTER: TRUTH TABLE

CLK	Q1	Q2	Q3	Q4
1	D1	-	-	-
2	D2	D1	-	
3	D3	D2	D1	-
4	D4	D3	D2	D1
5	D5	D4	D3	D2
6	D6	D5	D4	D3
7	D7	D6	D5	D4
…				

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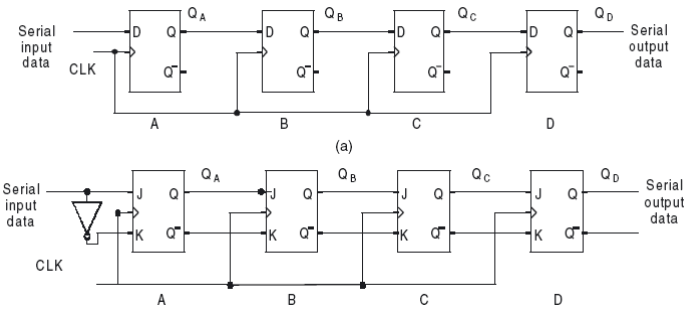
SHIFT-RIGHT REGISTER



In the shift register using D flip-flop, D input of the left most flip-flop is used as a serial input line. To input 0, one should apply 0 at the D input and vice versa. The clock pulse is applied to all the flip-flops simultaneously. When the clock pulse is applied, each flip-flop is either set or reset according to the data available at that point of time at the respective inputs of the individual flip-flops.

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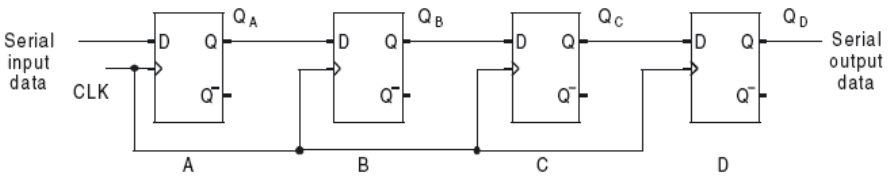
SHIFT-RIGHT REGISTER



Timing pulse	Q_A	Q_B	Q_C	Q_D	*Serial output at* Q_D
Initial value	0	0	0	0	0
After 1st clock pulse	1	0	0	0	0
After 2nd clock pulse	1	1	0	0	0
After 3rd clock pulse	0	1	1	0	0
After 4th clock pulse	1	0	1	1	1

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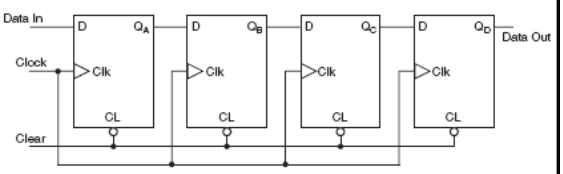
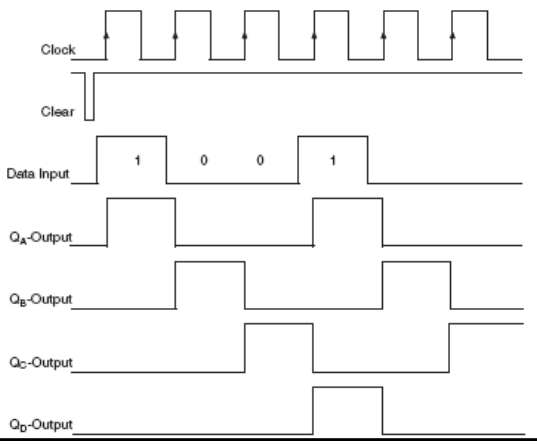
SHIFT REGISTER OPERATION

Serial-in serial-out shift register



Timing waveforms



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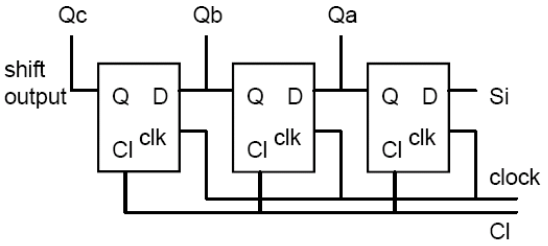
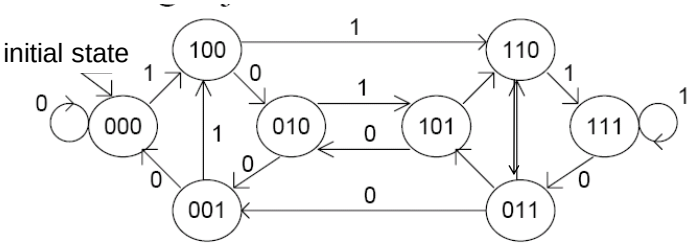
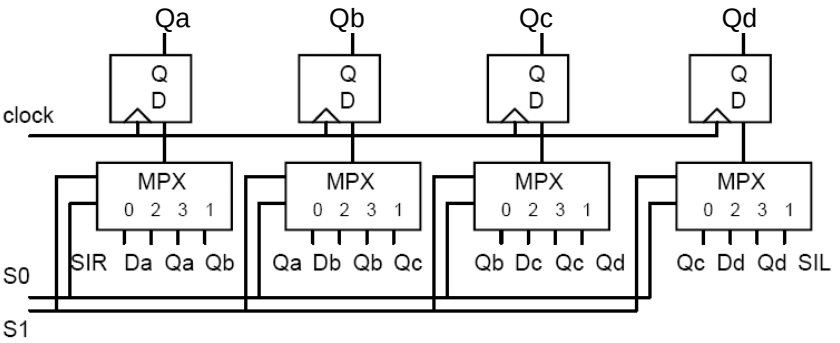
SHIFT REGISTER: STATE TRANSITION DIAGRAM



State transition diagram



BI-DIRECTIONAL SHIFT REGISTER



S1	S0	
0	0	shift right (SHR)
0	1	shift left (SHL)
1	0	load (LOAD)
1	1	hold (HOLD)

Functional diagram of bi-directional shift register with load and hold facility

REGISTERS: DESIGN ASPECTS

Collection of flip-flops with similar controls and logic

Stored values somehow related (e.g. form binary value)

Share clock, reset, and set lines

Similar logic at each stage

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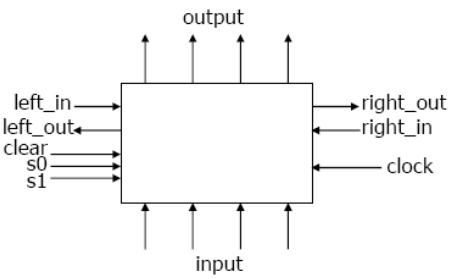
UNIVERSAL SHIFT REGISTER

- Holds 4 values
  - serial or parallel inputs
  - serial or parallel outputs
  - permits shift left or right
  - shift in new values from left or right



clear sets the register contents and output to 0

s1 and s0 determine the shift function

s0	s1	function
0	0	hold state
0	1	shift right
1	0	shift left
1	1	load new input

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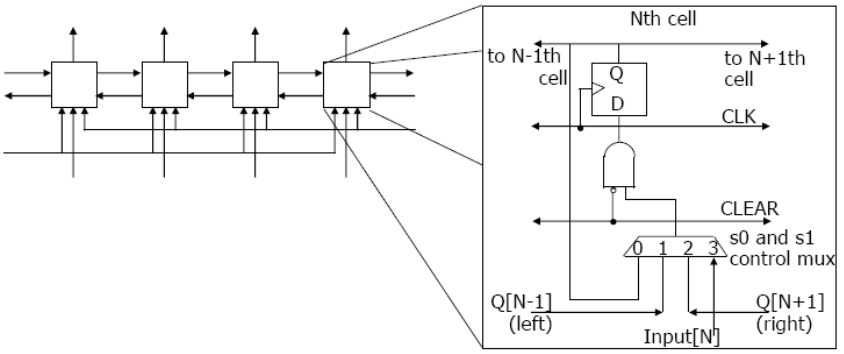
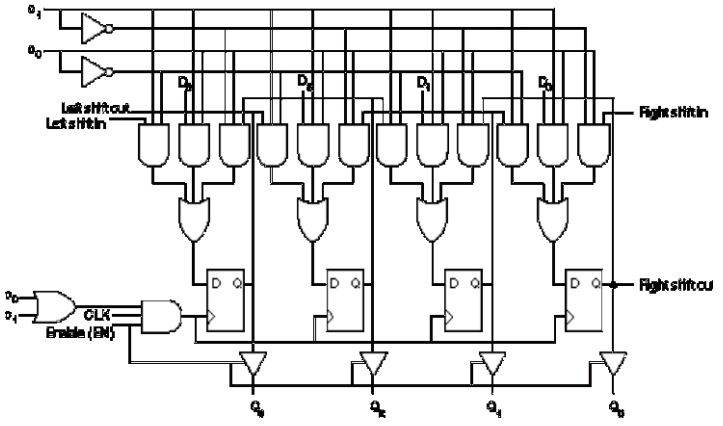
DESIGN OF UNIVERSAL SHIFT REGISTER

- Consider one of the four flip-flops
  - new value at next clock cycle:

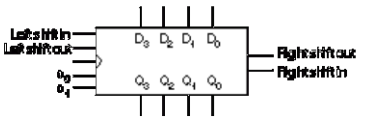
clear	s0	s1	new value
1	–	–	0
0	0	0	output
0	0	1	output value of FF to left (shift right)
0	1	0	output value of FF to right (shift left)
0	1	1	input



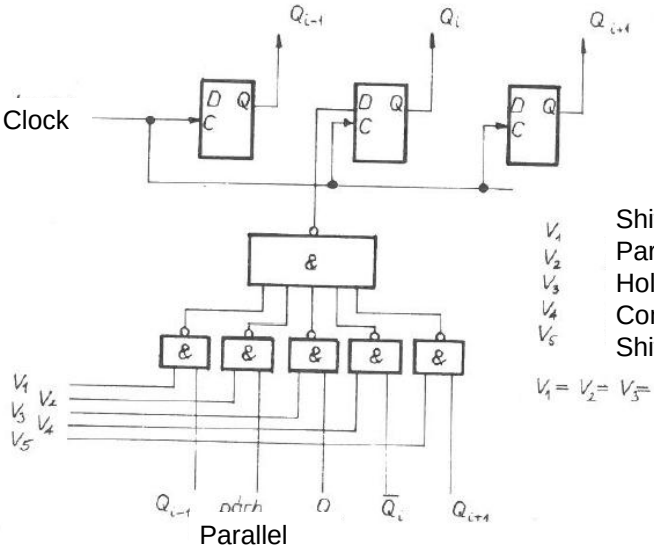
A LEFT-RIGHT SHIFT REGISTER WITH PARALLEL READ AND WRITE



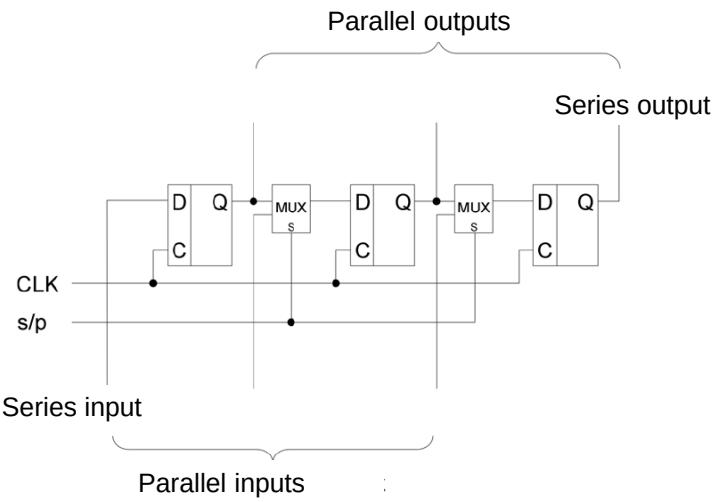
Control s_1	s_0	Function
0	0	No change
0	1	Shift left
1	0	Shift right
1	1	Parallel load



UNIVERSAL REGISTER



SERIES/PARALLEL INPUT/OUTPUT REGISTER



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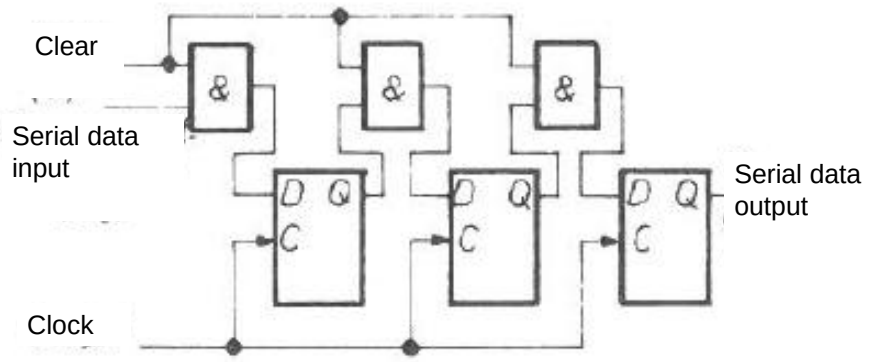
SHIFT REGISTER: SYNCHRONOUS CLEAR



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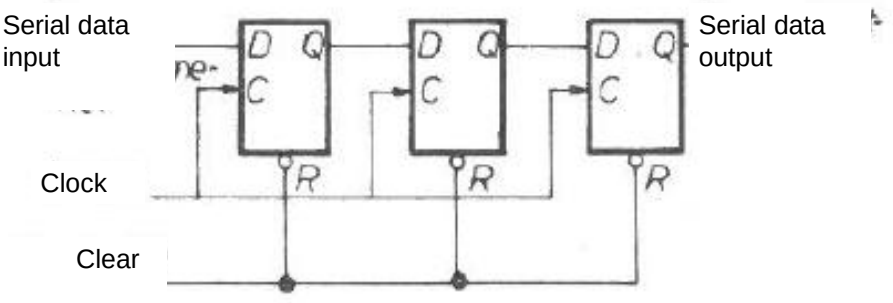
SHIFT REGSTER: ASYNCHRONOUS CLEAR



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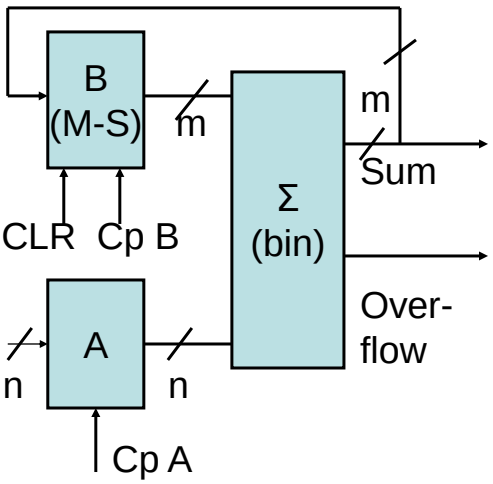
REGISTER APPLICATION

Serial addition of two numbers.



1. Clearing of register B (CLR B);
2. Loading first addend to register A (Cp A);
3. Result (sum) transferred into register B (Cp B);
4. Loading next addend to register A (Cp A);
5. Repeat 3. and 4. till there is a new addend.

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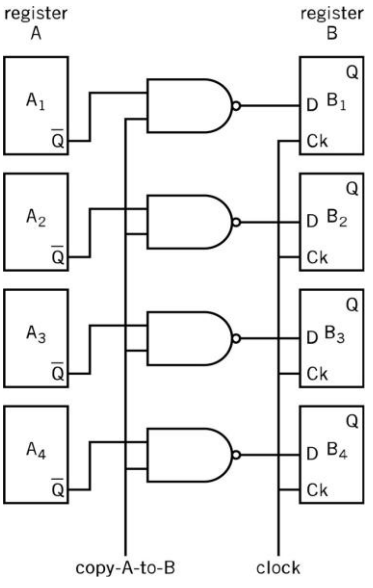
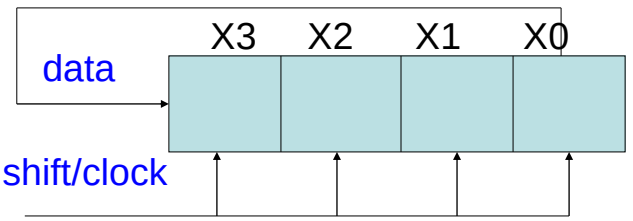
EXAMPLE: REGISTER COPY OPERATION

- Uses both sequential and combinatorial logic



CIRCULAR REGISTER (1)



A circular register is formed by connecting (feeding back) the output of the last flip-flop to the (D-) input of the first flip-flop. In the circular register the clock keeps the binary information rotating. The bit pattern can be loaded in a parallel way.

SHIFT REGISTER COUNTERS

Both counters and shift registers are some kinds of cascade arrangement of flip-flops. A shift register, unlike a counter, has no specified sequence of states. However, if the serial output of the shift register is fed back to the serial input, we do get a circuit that exhibits a specified sequence of states. The resulting circuits are known as *shift register counters.*

Generally they are not used to count pulses, but to generate special code sequences. Two types are common:

- n-bit direct/simple ring counter realizing n state (mod n counter);
- n-bit Johnson/Möbius counter, realizing 2n states (mod 2n counter).

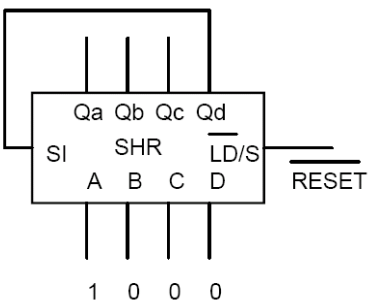
SHIFT REGISTER COUNTERS

Shift register counter – a circuit formed by a shift registers and combinational logic. The state diagram for this state machine is cyclic. This circuit does not necessarily count in ascending or descending order.

Ring counter – the simplest shift register counter. This circuit uses a *n*-bit shift register to obtain a counter with *n* states

RING COUNTER

The circular register can be operated as a ring counter. The counter is initially preset, e.g. by loading 1 into the first flip-flop. Then the *modulus* of the counter is equal to the number of flip-flops N. Appropriately changing the pre-loaded bit pattern, the *modulus* can be decreased.

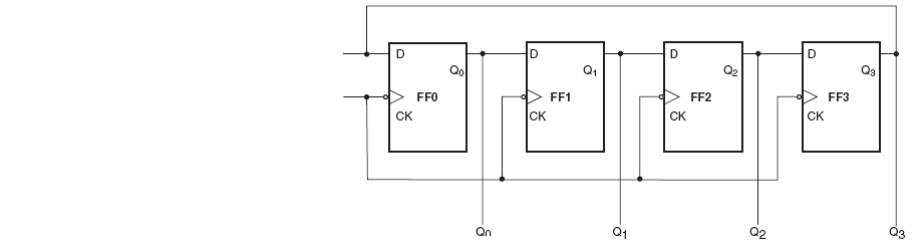


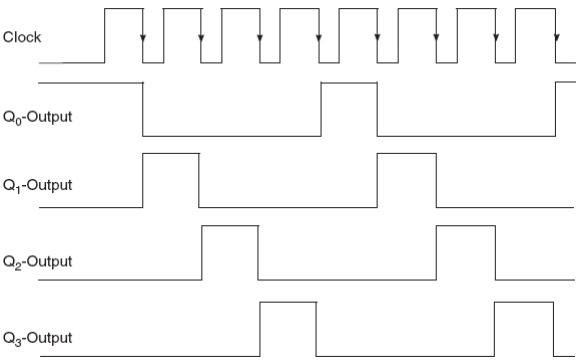
Encoding:

Qa	Qb	Qc	Qd
1	0	0	0
0	1	0	0
0	0	1	0
0	0	0	1

E.g. depending on the preloaded code word, an 4-bit ring counter can exhibit six different cycles.

4-BIT RING COUNTER OPERATION





Timing waveforms

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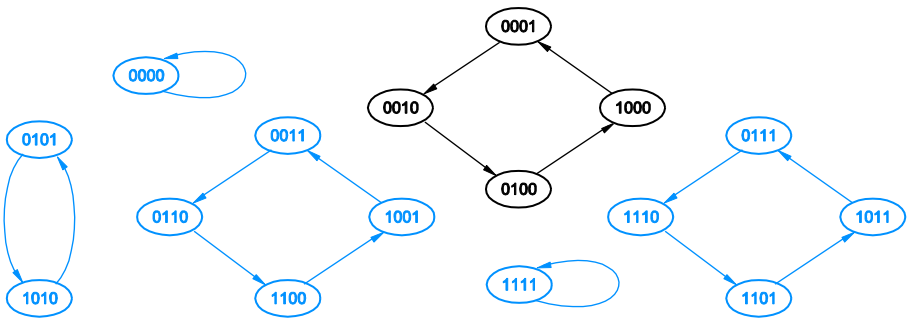
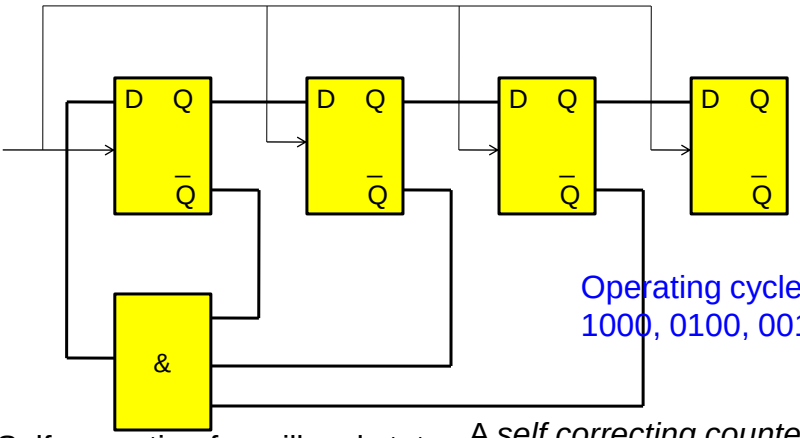
4-BIT RING COUNTER CYCLES



State transition diagram of the 4-bit ring counter: six possible cycles

SELF CORRECTING RING COUNTER

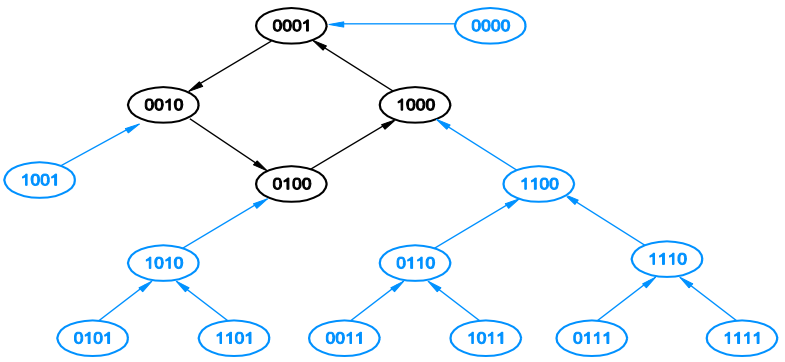


Operating cycle:
1000, 0100, 0010, 0001

Self correction from illegal state:
e.g. 1110⇒0111⇒0011⇒0001

A *self correcting counter* is designed so that all abnormal states have transitions leading to normal states.

SELF CORRECTING RING COUNTER



State transition diagram of the 4-bit self-correcting ring counter

RING COUNTER APPLICATIONS

Signal series generated by ring counter state can be used for control purposes.

Similar signal series can also be generated by a counter-decoder system, however in such case greater then one Hamming distance codes can be present on the decoder input. This can lead to the occurrence of functional hazards.

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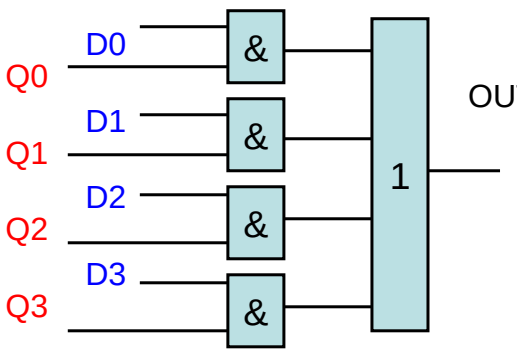
RING COUNTER APPLICATION

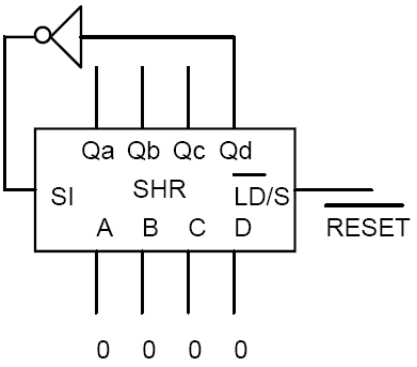
A ring counter, instead of counting with binary numbers, counts with words that have a single high bit. These are ideal for timing a sequence of digital operations.

An application: time-division multiplexor



JOHNSON (MÖBIUS) COUNTER

Twisted-ring, Möbius or Johnson counter is a n-bit shift register whose serial input receives the complement of serial output. This counter has 2n states.
The feedback circuit is a single inverter. Beginning from a state of full 0s, the counter at first fills up itself with 1s, then with 0s. The modulus is 2N.



Encoding:

Qa, Qb, Qc, Qd:

0000, 1000, 1100, 1110, 1111, 0111, 0011, 0001

JOHNSON COUNTERS

A Johnson counter is a special case of a shift register, where the output of the last stage is inverted and fed back to the first stage.

A pattern of bits equal to the length of the shift register thus circulates indefinitely.

These counters are sometimes called „walking ring” counters.

JOHNSON (MÖBIUS) COUNTER

State decoding: two-input AND gate and inverters.

E.g. 0000 (0) $\overline{Qa}\ \overline{Qd}$

1000 (1) $Qa\overline{Qb}$ etc.

The ouputs obtained in this way do not contain hazards, because the codes are one-step codes.

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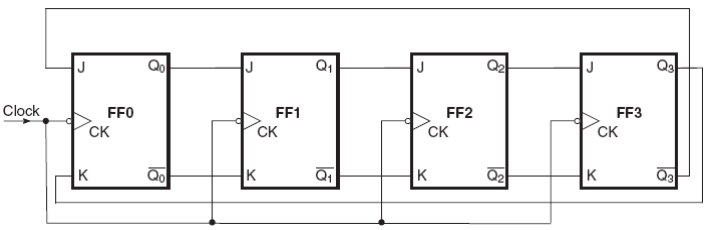
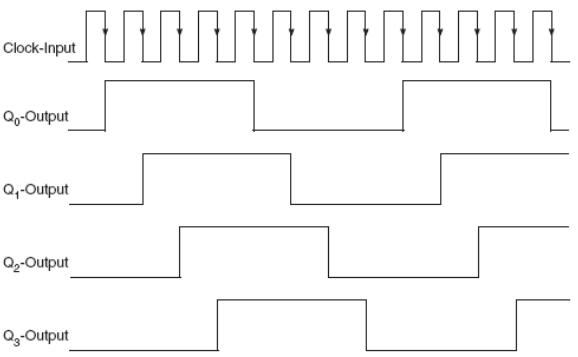
4-BIT JOHNSON COUNTER OPERATION





Timing waveforms

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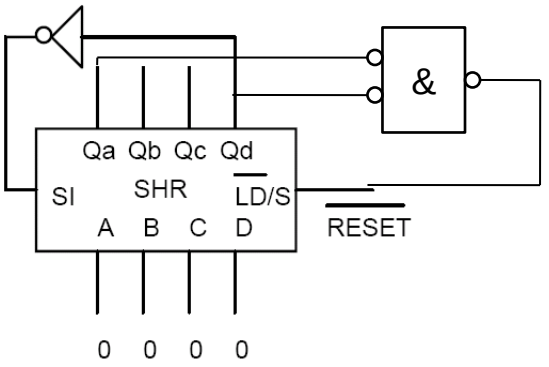
SELF-CORRECTING JOHNSON COUNTER

From any initial state returns to the normal cycle. Operation: The Johnson counter sooner or later takes up the state 0XX0. This activates the LOAD function, setting the normal operation cycle.



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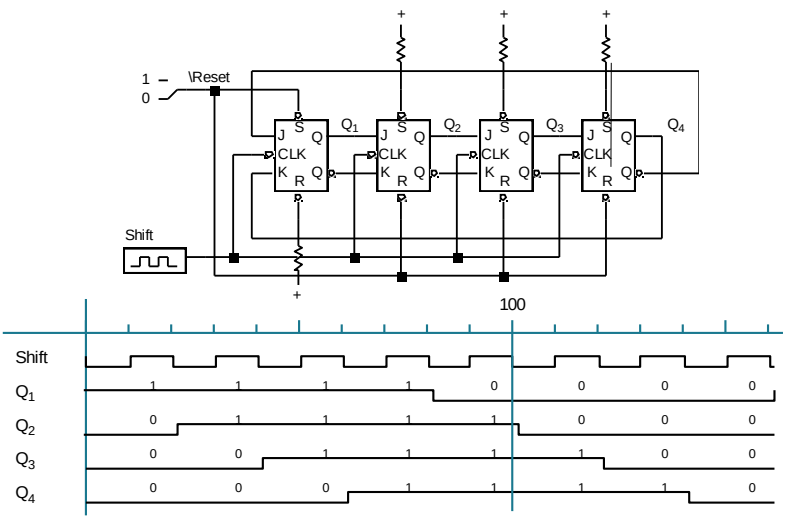
JOHNSON COUNTER



8 possible states, single bit change per state, useful for avoiding glitches (hazards)

STRAIGHT AND TWISTED RING COUNTERS

Four-bit ring counter sequences

Straight ring/*Overbeck counter*					Twisted ring/*Johnson counter*				
State	Q0	Q1	Q2	Q3	State	Q0	Q1	Q2	Q3
0	1	0	0	0	0	0	0	0	0
1	0	1	0	0	1	1	0	0	0
2	0	0	1	0	2	1	1	0	0
3	0	0	0	1	3	1	1	1	0
0	1	0	0	0	4	1	1	1	1
1	0	1	0	0	5	0	1	1	1
2	0	0	1	0	6	0	0	1	1
3	0	0	0	1	7	0	0	0	1
0	1	0	0	0	*0*	0	0	0	0

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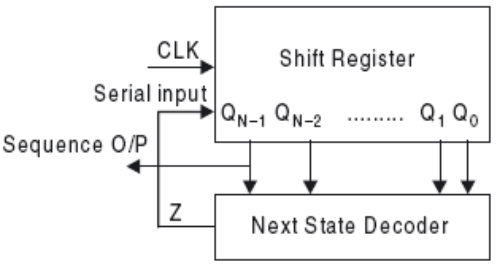
SEQUENCE GENERATOR

A sequence generator is a circuit that generates a desired sequence of bits in synchronization with a clock. A sequence generator can be used as a random bit generator, code generator, and prescribed period generator. The block diagram of a sequence generator is shown here.



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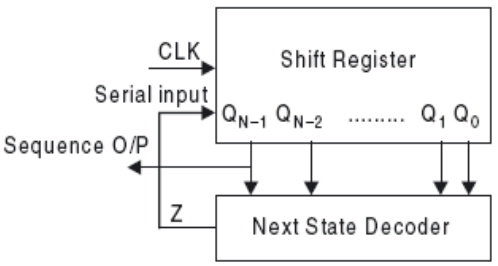
SEQUENCE GENERATOR



The sequence generator can be constructed using shift register and a next state decoder. The output of the next state decoder (Z) is a function of QN-1, QN-2,……Q1, Q0 and is connected to the serial input of the shift register. This sequence generator is similar to a ring counter or a Johnson counter.

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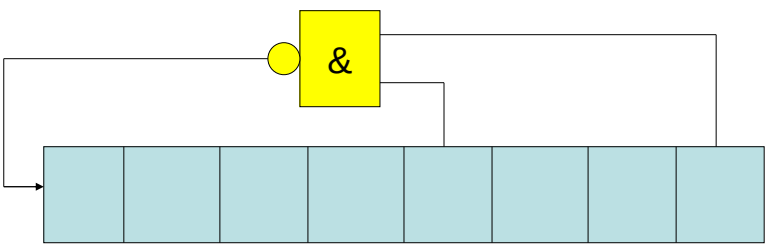
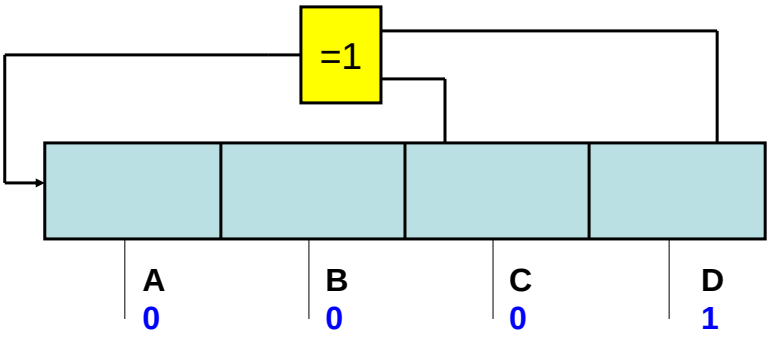
CIRCULAR REGISTER (2)



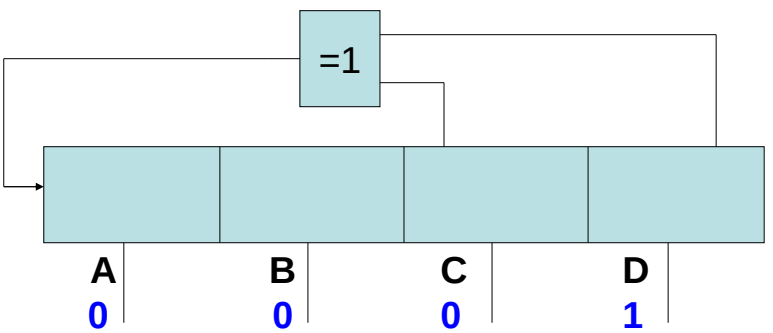
The 8-bit circular register has 12 states with the feedback shown. Starting form the state 000...0, after the 4th then after the 16th clock cycle its state will be 11110000.

CIRCULAR REGISTER (3): PSEODO RANDOM NUMBER GENERATOR



If the feedback network is an XOR gate, then using appropriate outputs of the register, the modulus of the counter will be 2^N -1.
For the circuit shown, with the given initial value the modulus will be the maximum possible i.e.15.

PSEUDO RANDOM NUMBER GENERATOR



Sequence:
(1) 0001, (8) 1000, (4) 0100, (2) 0010, (9) 1001,
(12) 1100, (6) 0110, (11) 1011, (5) 0101, (10) 1010,
(13) 1101, (14) 1110, (15) 1111, (7) 0111, (3) 0011.
Important property: the sequence of codes is rather random.
(c.f. Benesóczky Z., Digitális tervezés funkcionális elemekkel)

PSEUDO RANDOM NUMBER GENERATOR

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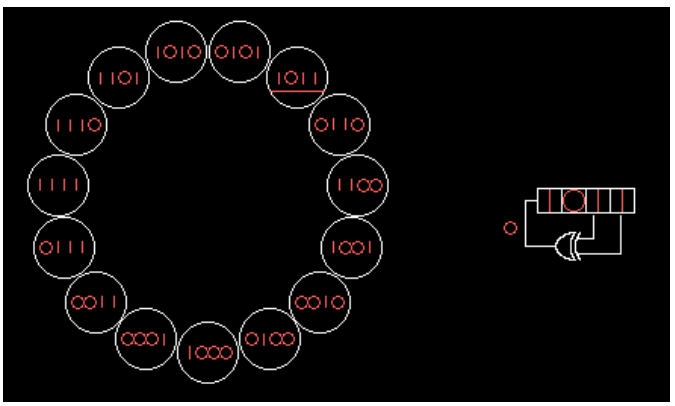
No. of stages	No. of states	Serial No. of FFs to fed back
3	7	3, 2
4	15	4, 3 (shown above)
5	31	5, 3
6	63	6, 5
7	127	7, 6

(c.f. Benesóczky Z., Digitális tervezés funkcionális elemekkel ...)

4-BIT FIBONACCI LFSR



A 4-bit Fibonacci LFSR with its state diagram. The XOR gate provides the feedback that shift bits left to right. The maximum sequence consists of every possible state except rhe 0000 state.

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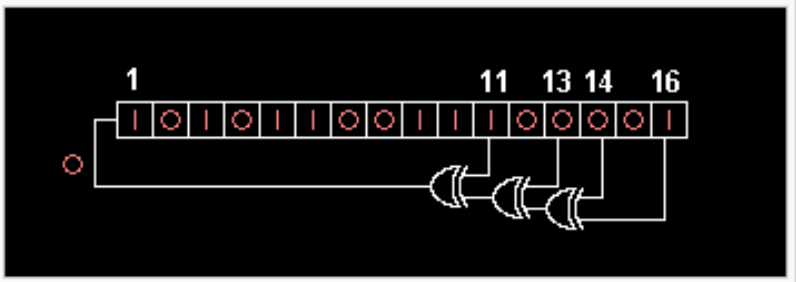
16-BIT FIBONACCI LFSR



A 16-bit Fibonacci LFSR. The feedback tap numbers in white correspond to a primitive polynomial in the table so the register cycles through the maximum number of 65535 states excluding the all-zeroes state. The state ACE1 hex shown will be followed by 5670 hex.

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REVIEW QUESTIONS

1. A shift register has seven fl ip-fl ops. What is the largest binary number that can be stored in it? Octal number? Decimal number? Hexadecimal number?

2. The content of a 4-bit register is initially *1011*. The register is shifted 7 times to the right with the serial input being *1010110*. What is the content of the register after each shift?

3. Draw the circuit for a universal shift register and explain its operation. Draw the circuit for a universal shift register and explain its operation.

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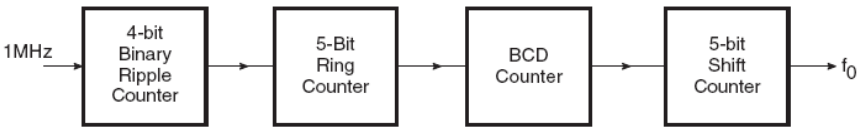
PROBLEMS AND EXERCISES

1. For the multistage counter arrangement shown below determine the frequency of the output signal.



(ANS: 125 Hz)

2. A four-bit ring counter and a four-bit Johnson counter are in turn clocked by a 10 MHz clock signal. Determine the frequency and duty cycle of the output of the output flip-flop in the two cases.

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PROBLEMS AND EXERCISES

3. Construct a Johnson counter for twelve timing sequences.

4. Design a 6-bit ring counter using J-K flip-flops.

5. Refer to the logic circuit below. Determine the modulus of this counter and write its counting sequence.