DIGITAL TECHNICS II

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6. LECTURE: LOGIC CIRCUITS I

2nd (Spring) term 2017/2018

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6. LECTURE
LOGIC CIRCUITS I

1. Digital/logic circuit families

2. The inverter and its properties

3. Transistor-Transistor Logic (TTL) : integrated bipolar junction transistor (BJT) logic circuits

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BASIC DIGITAL CIRCUITS

- Logic circuits – homogeneous building blocks with unified (common) properties
- Gates, flip-flops, etc. – common supply voltage, common logic levels, similar propagation delays, etc.
- Technology – common, integration on one chip

Logic circuit families

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LOGIC FAMILIES

- Different devices use different voltages ranges for their logic levels
- They also differ in other characteristics
- In order to assure correct operation when gates are interconnected they are normally produced in families
- The most widely used families are:
  - **complementary metal oxide semiconductor (CMOS)**
  - **transistor-transistor logic (TTL)**
  - **emitter-coupled logic (ECL)**

BASIC DIGITAL CIRCUITS: THE INVERTER

• From the point of view of construction the fundamental element of the logic family is the inverter

• The inverter determines the basic properties of the logic circuits:
  - logic levels,
  - noise margins,
  - propagation delays,
  - power dissipation.

• The other logic components/gates can be derived from the inverter, e.g.
  - NOR, NAND gates: inverter with extension
  - SR flip-flop: two NOR gates, etc.

Gates are inverters in disguise!

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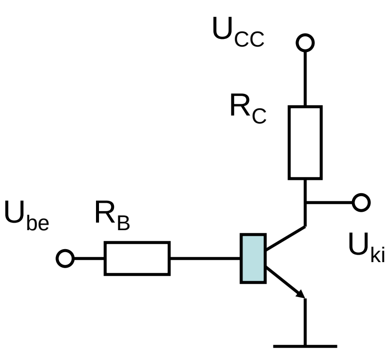
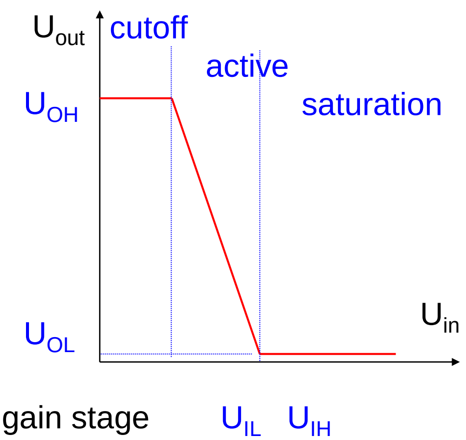
BASIC INVERTER CIRCUIT





Basically a common-emitter gain stage operated in cutoff or in saturation.

$U_{in} = 0$ V $\quad U_{out} \approx U_{supply}$

$U_{in} \approx U_{supply} \quad U_{out} \approx 0$ V

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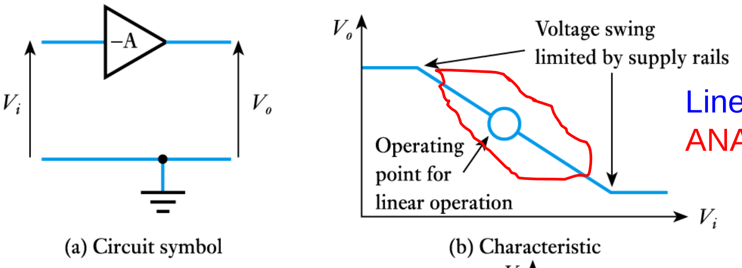
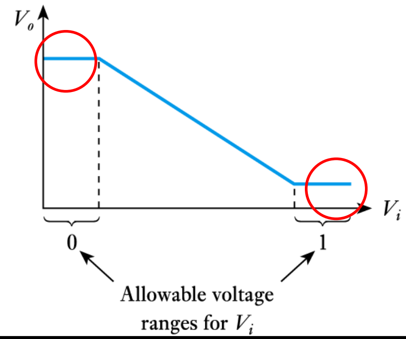
180º PHASE SHIFT AMPLIFIER AND INVERTER



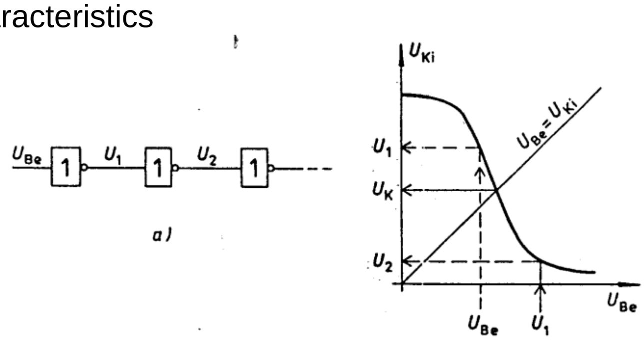
Linear operation
ANALOGUE

Inverting operation
DIGITAL



FUNCTIONS OF INVERTERS

- Signal restoring – active region of transfer characteristics, gain/amplification
- Noise rejection – small slope regions of the transfer characteristics



If the transfer characteristics is steep, the inverters (e.g. series connection) restore the digital signal levels.

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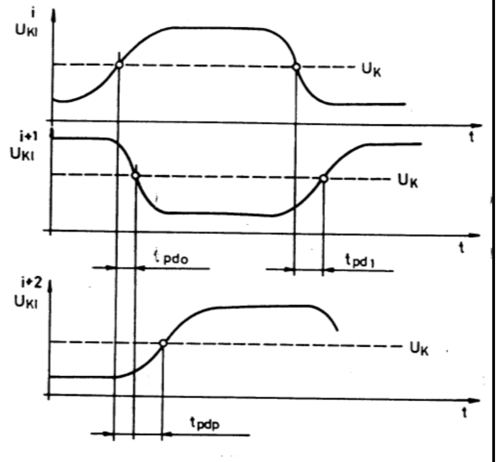
PROPAGATION DELAY

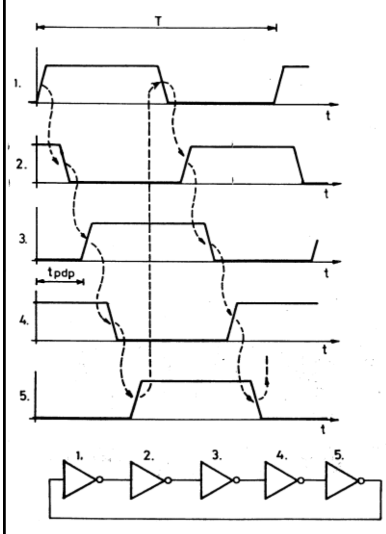
Propagation delay
Time elapsed between the appearance of input and output signal. It is different for up- and down-going signal. (Defined between 50 percent signal levels.)

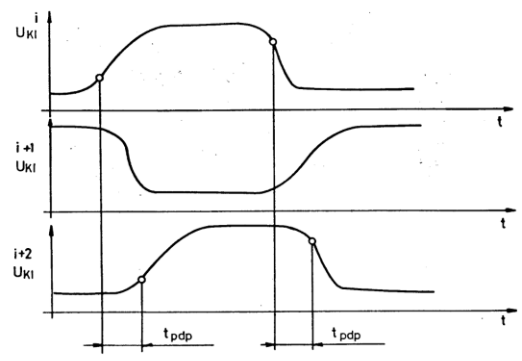
Pair propagation delay
In a long inverter chain (e.g. ring-oscillator) the signal shapes of every second inverter are the same. This defines the pair propagation delay.



RING OSCILLATOR

Ring oscillator: odd number of inverters.
The oscillation period: $T=Nt_{pdp}$





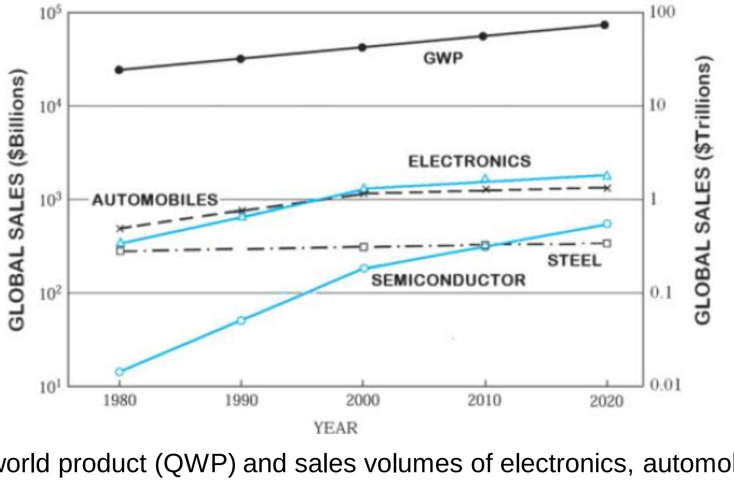
Signal shapes in an N = 5 ring oscillator.

HISTORY OF DIGITAL ELECTRONICS

The design of digital circuits has progressed from resistor-transistor logic (RTL) and diode-transistor logic (DTL) to transistor-transistor logic (TTL) and emitter-coupled logic (ECL) to complementary MOS (CMOS)

The density and number of transistors in microprocessors has increased from 2300 in the 1971 4-bit 4004 microprocessor to 25 million in the more recent IA-64 chip and it is projected to reach over one billion transistors by 2010.

ELECTRONICS: GLOBAL RELEVANCE



Gross world product (QWP) and sales volumes of electronics, automobile, semiconductor and steel industries form 1980 to 2010 and projected to 2020.

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ELECTRONICS: GLOBAL RELEVANCE

The figure shows the sales volume of the semiconductor-device–based electronics industry in the past 30 years and projects sales to the year 2020. Also shown are the gross world product (GWP) and the sales volumes of the automobile, steel, and semiconductor industries. We note that the electronics industry surpassed the automobile industry in 1998. If the current trends continue, in year 2020 the sales volume of the electronics industry will reach two trillion dollars and will constitute about 3% of GWP. It is expected that the electronic industry will remain the largest industry in the world throughout the 21st century. The semiconductor industry, which is a subset of the electronic industry, will surpass the steel industry around 2010 and constitute 25% of the electronics industry in 2020.

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THE AGE OF SILICON

It has been said the silicon is to electronics what steel is to mechanical engineering.

Periodizations of the 20th century:

1st half: age of carbon and steel,
2nd half: age of silicon

Before and after the transistor (invented in 1947)

Before and after Shockley

William Bradford Shockley (1910-1989)
Physics Nobel 1956

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MOORE’S LAW

The development of complexity and performance of silicon devices is unparalelled in the history of technology. Never before could improvements be measured in terms of logarithmic scale for   such a sustained period. This is often seen as the embodiment of „Moore’s Law”.

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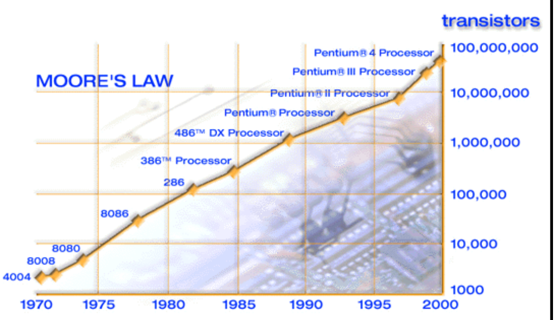
MOORE’S LAW

Gordon Moore (co-founder of Intel) predicted in 1965, just four years after the first planar integrated circuit was discovered, that the number of transistors per integrated circuit would double every 18 months.

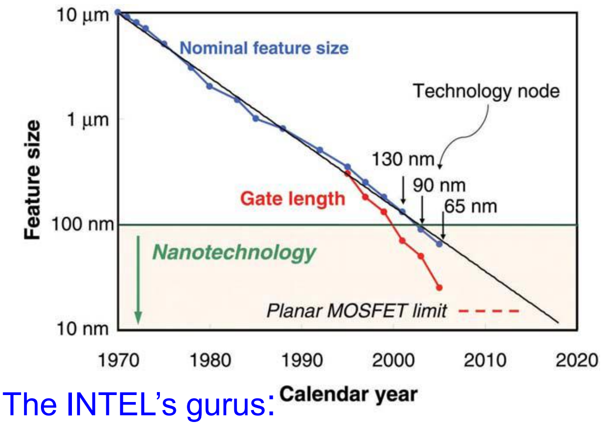
He forecast that this trend would continue through 1975.

Moore's Law has been maintained for far longer, it has become a universal law of the entire semi-conductor industry. It still holds true as we enter the second decade of new century.



Moore’s law is about human ingenuity not physics.

MOORE'S LAW

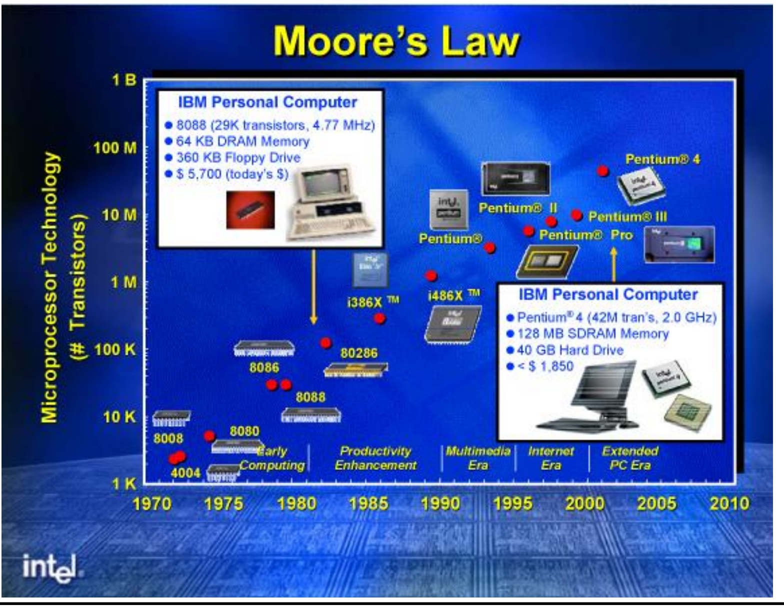


The INTEL's gurus:

A. Groove, R. Noyce
G. Moore INTEL,1970

Robert NOYCE the visionary (co-invertor of IC)
Gordon MOORE the virtuoso of technology
Andrew GROVE (*GRÓF András*) the technologist turned scientist
Logic technology node and transistor gate length versus calendar year.
Note:
mainstream Si technology is nanotechnology.

MOORE'S LAW



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FINANCE

Cost (investment) of an IC fab

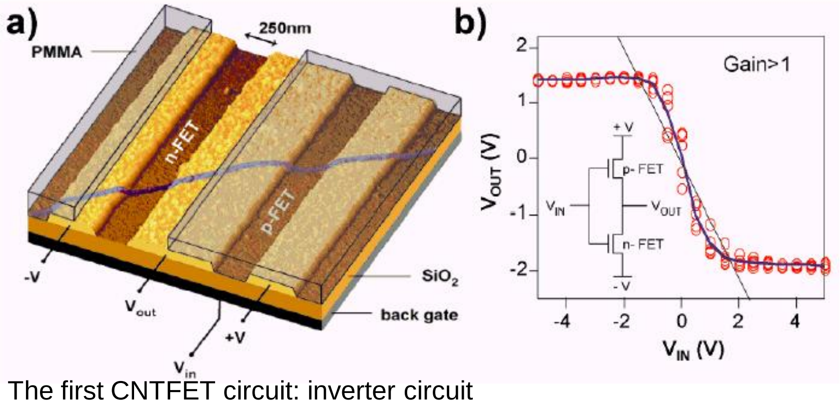
1999: 5.000.000.000 $

2010: 50.000.000.000 $ = 12.000 billion HUF!
(Hungary's yearly budget….)

Solution: fabs only at few places …
design at a great lot of places …

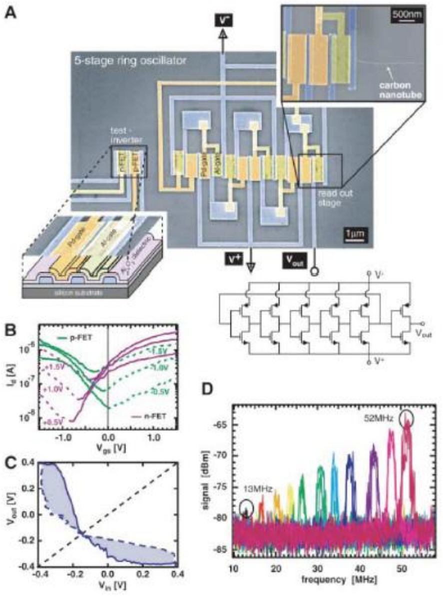
WINDOW INTO THE FUTURE (?):

CNT FET INVERTER AND LOGIC GATES



The first CNTFET circuit: inverter circuit
(red circles : results of five measurement series)

CNT RING OSCILLATOR

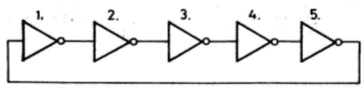


An Integrated Logic Circuit Assembled on a Single Carbon Nanotube

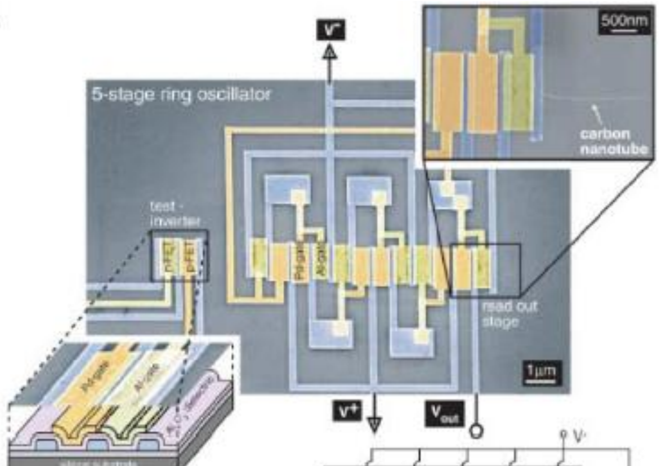
Zhihong Chen,[1] Joerg Appenzeller,[1*] Yu-Ming Lin,[1] Jennifer Sippel-Oakley,[2] Andrew G. Rinzler,[2] Jinyao Tang,[3] Shalom J. Wind,[4] Paul M. Solomon,[1] Phaedon Avouris[1*]

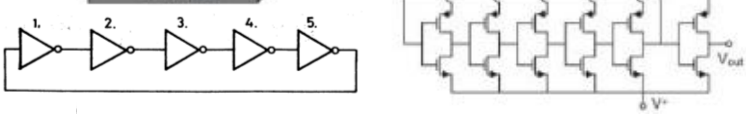
www.sciencemag.org SCIENCE VOL 311 24 MARCH 2006

Fig. 1. (**A**) Scanning electron microscope image of a SWCNT ring oscillator consisting of five CMOS inverter stages. A test inverter was added to determine the parameter set for the actual measurement. (**B**) Characteristics for the p-type FET with Pd metal gate and n-type FET with Al gate. (**C**) Inverter characteristics and its mirrored curve. (**D**) Voltage-dependent frequency spectra. From the left to the right, the respective supply voltages are as follows: V_{dd} = 0.5 V and 0.56 V to 0.92 V (in 0.4-V increments).



CNT RING OSCILLATOR





LOGIC CIRCUITS GENERATIONS AND FAMILIES

The circuit technologies are the relevant factors which determine and characterize the generations of logic circuits.

A logic family of monolithic digital integrated devices is a group of electronic logic gates, flip-flops, etc., constructed using one of several different designs and technology, usually with compatible logic levels and power supply characteristic within the family.

Before the widespread use of integrated circuits, various vacuum-tube and solid-state logic systems were in use, but these were never as standardized and interoperable as the IC devices.

LOGIC CIRCUIT GENERATIONS (1)

1930s, relay circuits, Bell Labs
(driving force: telephone exchange switching)

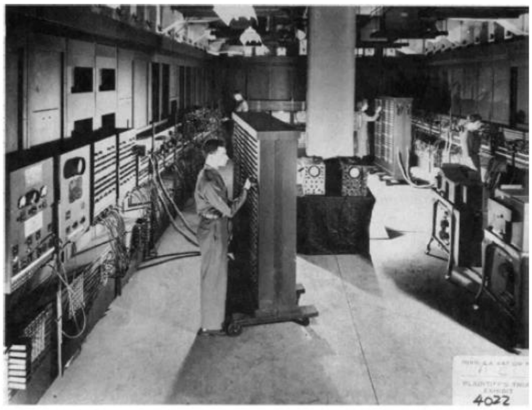
1940s, vacuum tubes e.g. ENIAC, built in 1946 (electronic numerical integrator and calculator), calculated the trajectory of an artillery shell in only 30 sec. Large and expensive…

18 thousand vacuum tubes
60 thousand pounds (27 thousand kg)
16200 cubic feet (480 m^3)
174 kW

(c.f. four-operation hand-held calculator appr. 9 000 transistors)

(driving force: military applications, artillery shell trajectory calculations)

ENIAC: 1946



Further comment: Failure rate of a commercial vacuum tube is about 1/2000 per hour, of an industrial or high-reliability type is about 10 times smaller.
Estimated failure rate of the ENIAC **about one per hour (!)**

TRANSISTOR AND IC

Perhaps the invention which determined the 20th century the greatest manner.

Two transistor concepts:

to control the flow of electrons by external field: field effect transistor (FET, MOSFET, etc.)

to create inside the material (semiconductor) the ”control electrode”: bipolar junction transistor

FET	Field Effect Transistor
MOS	Metal-Oxide-Semiconductor
BJT	Bipolar Junction Trasistor
TRANSISTOR	TRANSfer resISTOR

LOGIC CIRCUIT GENERATIONS (2)

1950/1960 semiconductor diode and transistor circuits

- RTL resistor-transistor-logic
- DTL diode-transistor-logic
- ECL emitter-coupled logic (later)

From 1961 SSI (above listed on one chip)

1960s TTL (transistor-transistor logic), Sylvania, then Texas Instruments, the TI system later became the *de-facto* industry standard

After 1960/1970: MOS metal oxide semiconductor : pMOS (1960s) then nMOS (1970s)

1980s CMOS (complementary metal-oxide-semiconductor) introduced in 1968 by RCA

TRANSISTOR-TRANSISTOR LOGIC: INTRODUCTION

Mostly widely used IC technologies.

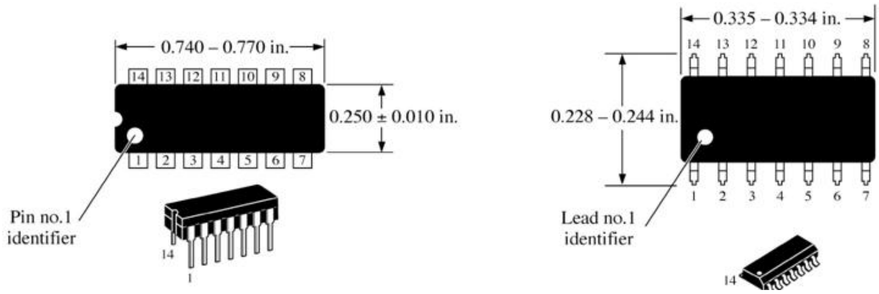
First circuit family: Texas Instruments
Semiconductor Network

74 Series (standard)& 54 Series (military specification)
Combination of BJTs, diodes, and resistors.
Implement logic function, e.g., NAND, NOR, etc.
Package (DIP, SMT)

The TTL system is based on the silicon bipolar transistor technology. It is a so called „saturation” logic system, because the transistors are driven to saturation or near-saturation

TTL: AN INTRODUCTION

- One of the commonest IC tecnology (bipolar)
- Two basic version 74 (commercial) and 54 (military)
- Several sub-series
- Bipolar transistors, diodes and resistors
- Packages: DIL, SMT



DIL — Dual-In-Line
SMT — Surface Mounting Technology

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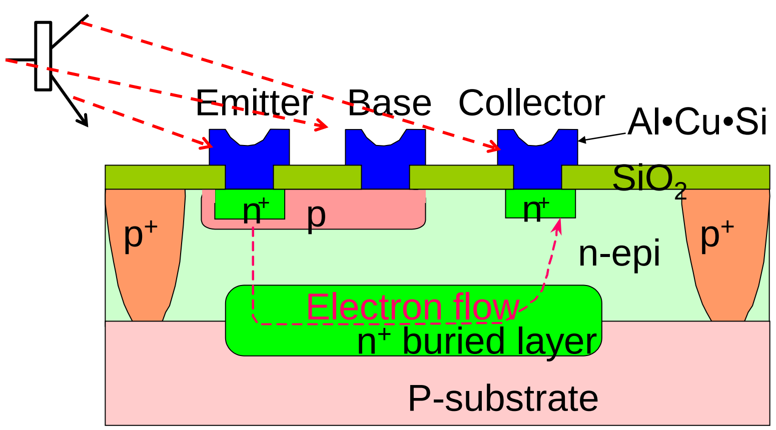
Si NPN (PLANAR) TRANSISTOR



The workhorse of the bipolar ICs is the Si npn transistor

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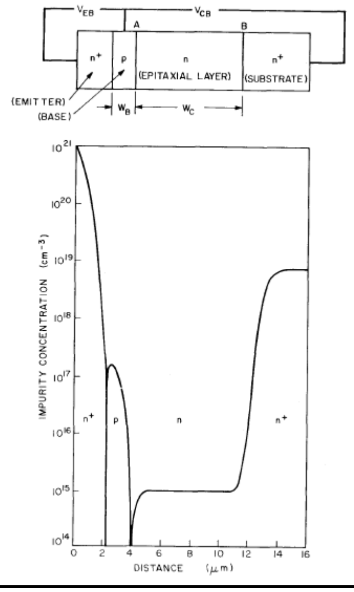
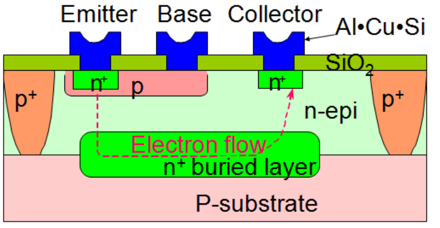
Si NPN (PLANAR) TRANSISTOR





IC: Si BIPOLAR TECHNOLOGY

- Technology optimization: to optimize the Si npn transistor.
- Components: bipolar transistor, diode, resistor, capacitor.
- Transistor (and all other components) in-plane structure – planar technology.

IC: THE Si BIPOLAR TRANSISTOR

• Typical dimensions:
emitter diffusion ~(2-2.5) μm
base diffusion ~4 μm
n-epitaxial layer (collector) ~10 μm
emitter window (small current transistor, ~1 mA)
(10-15) x (10-15) μm

E.g. in a TTL circuit one emitter is 16 x 16 μm, the nominal input current is max 1.6 mA (current density 6.25 A/mm^2).

Fig. 13 300 mm (12 in.) ingot and polished silicon wafers

300 mm (12 in.) ingot and polished silicon wafers

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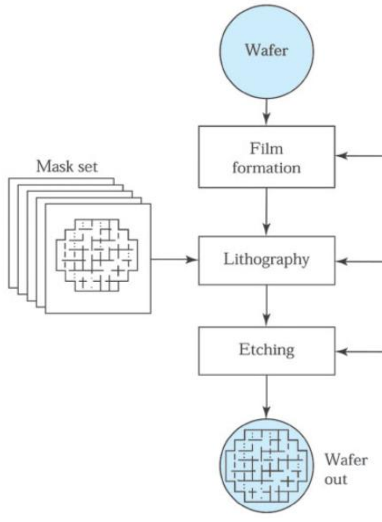

Schematic flow diagram of IC fabrication

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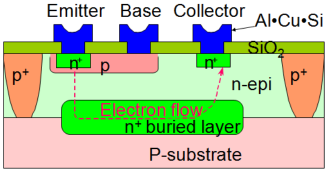
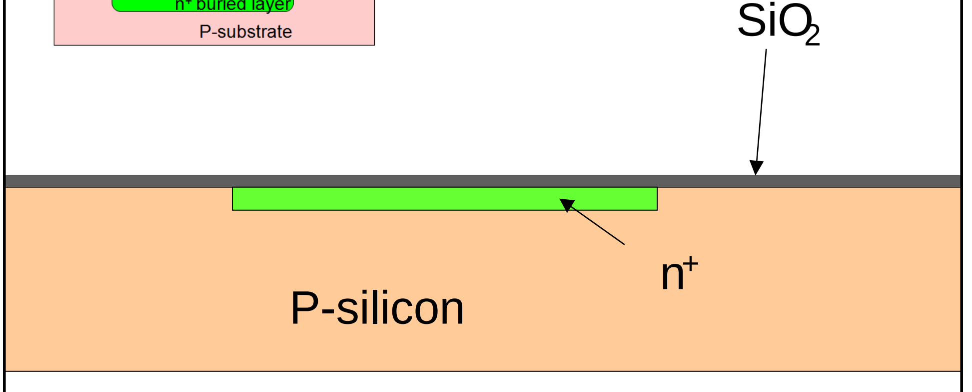
BURIED LAYER IMPLANTATION





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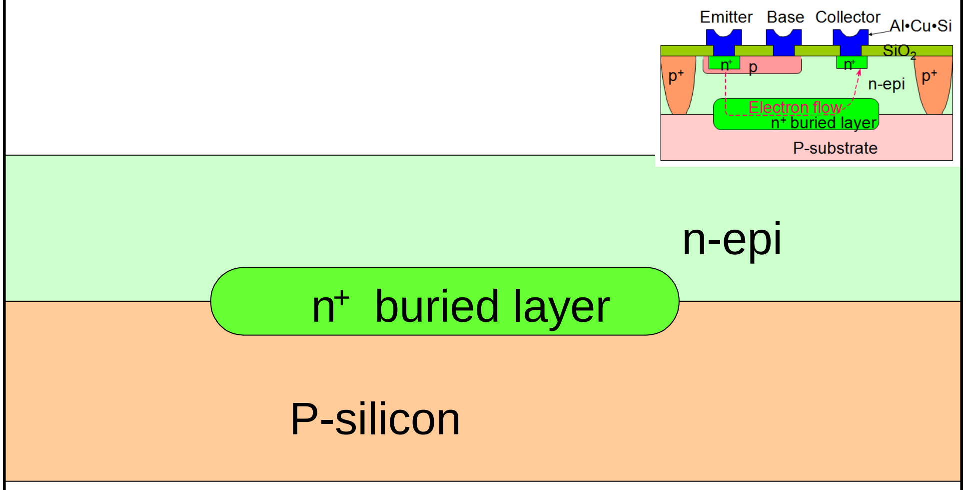
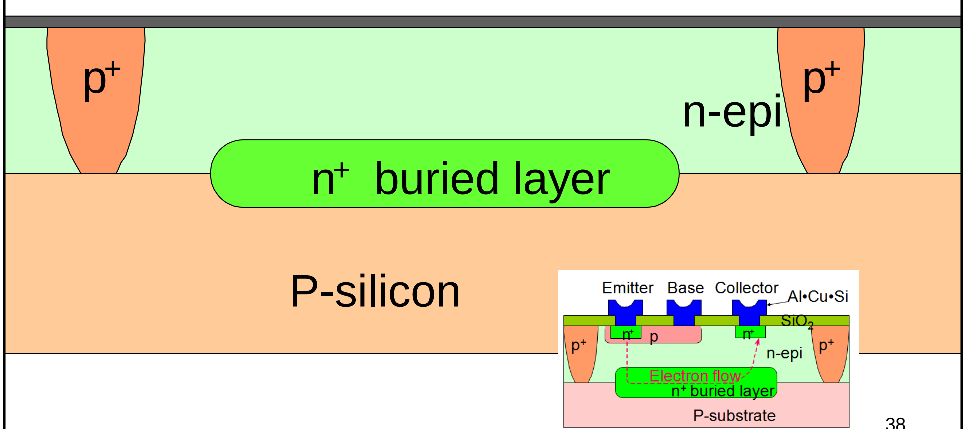
EPITAXY GROWTH



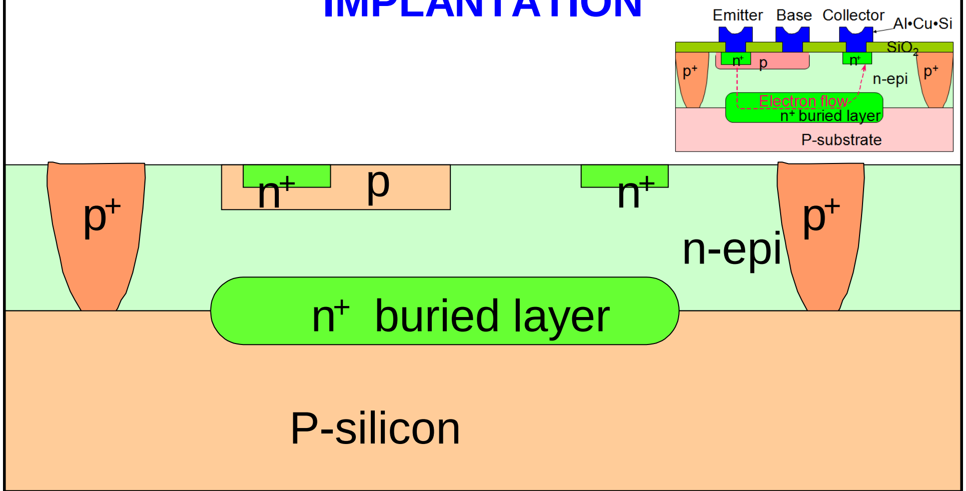
Growth of n-Si epitaxial layer

ISOLATION IMPLANTATION

P-type implantation (isolation)



EMITTER/COLLECTOR AND BASE IMPLANTATION



Formation of emitter and base regions and of collector contact region.

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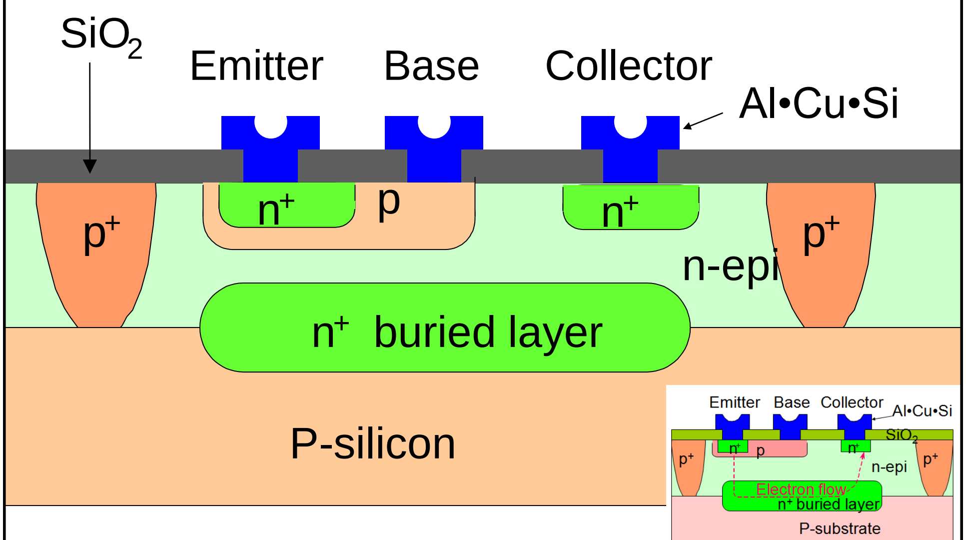
METAL DEPOSITION AND ETCHING



Deposition of contact and wiring metal layer, and patterning

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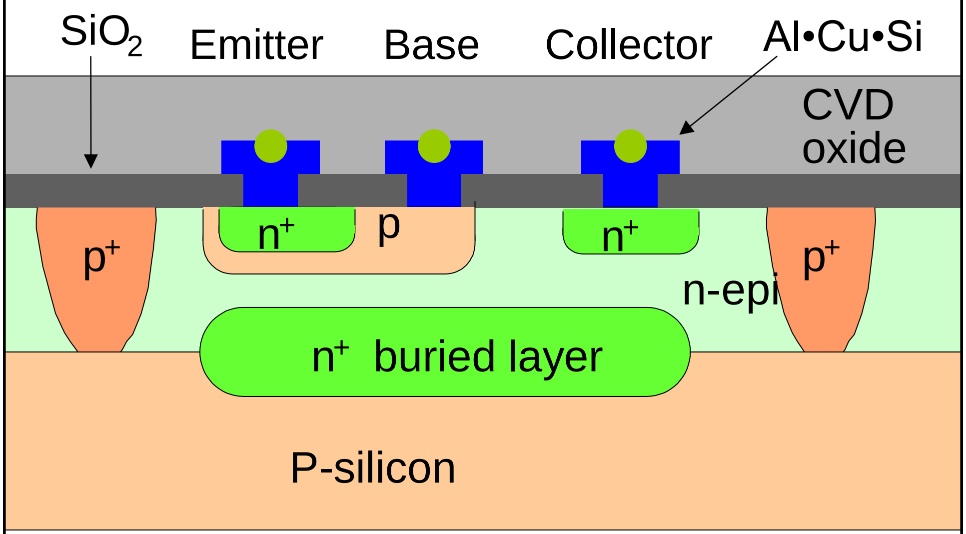
PASSIVATION OXIDE DEPOSITION



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IC: THE Si BIPOLAR TRANSISTOR

Typical Si npn transistor parameters

Region	V_{BE} (V)	V_{CE} (V)	Current Relation
Cutoff	< 0.6	Open circuit	$I_B=I_C=0$
Active	0.6-0.7	> 0.8	$I_C = h_{FE} I_B$
Saturation	0.7-0.8	0.2	$I_B \geq I_C/h_{FE}$

THE (BIPOLAR) TRANSISTOR

Probably no single development of modern physical science has touched so many people's lives so directly as has world-shaking invention of the transistor.
Xmas 1947: Bell scientists realized the world's first successful solid-state amplifier.
The transistor revolutionized electronic communication devices, as well as making practical the extensive development of high-speed, high-capacity computers. In regard to the latter, an important feature of the transistor is the low amount of energy required per bit of information processed and its extremely long operational life.
Its invention was truly a landmark, and it is small wonder that a Nobel prize of physics was awarded in 1956 to the men primarily responsible: John Bardeen, Walter Brattain, and William Shockley.

TRANSISTOR STORY: MILESTONES

- 1925-1928 J. E. Lilienfeld, field effect transistor patents
- 1947 J. Bardeen, W. H. Brattain (Bell Labs), point contact transistor (physics Nobel prize1956)
- 1948 W. Shockley (Bell Labs), pn junction, bipolar transistor (physics Nobel prize, 1956)
- 1958-1959 J. Kilby (Texas Instruments) integrated circuit (physics Nobel prize, 2000)
- 1958-1961 R. Noyce (Fairchild) integrated circuit (he did not live long enough for the Nobel prize…)

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TRANSISTOR HISTORY

1. Prehistoric times (i.e. BS-Before Shockley)

The first forty years of the twentieth century witnessed the discovery of quantum mechanics, the photon, electroluminescence, the role of defects in solids and the properties of metal-semiconductor contacts, all of which laid the foundation for the technological revolution that was to come. Quantum theory explained the difference between metals, semiconductors and insulators in terms of energy band-structure, and accounted for electron states associated with lattice defects and impurities. In 1934 Fermi invented pseudopotentials, which were to become vital for band-structure calculations. Schottky and Mott, separately described the metal-semiconductor contact in 1938, an understanding that was to become crucial to devices like MESFETs, MOSFETs, IMPATTs and charge coupled devices. Semiconductors began to be used as thyristors and photodetectors and point-contact rectification was beginning to be understood.
And then there was Shockley...

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2. History

Modern electronics began with the invention of the transistor at Bell Telephone Laboratories in Murray Hill, New Jersey by Bardeen, Brattain and Shockley who were subsequently awarded the Nobel Prize in 1956. The early transistors were chunky, centimetre-sized single crystals of Ge with p-n junctions back to back involving both electrons and holes. The physics of p-n junctions was set out in a classic paper by Shockley in 1949, the first example of what was to become a very fruitful interplay of physics and device technology. Shockley went on to contemplate the effect of heterojunctions (1951) and the advent of the junction field-effect transistor (JFET) (1952), innovations that had to wait a number of years for crystal-growing techniques to catch up with theory. At present time, field-effect transistors based on Si have revolutionized electronics and heterojunctions based on GaAs have found extensive roles in hot-electron transistors, photodetectors and, of course, in quantum-well devices.

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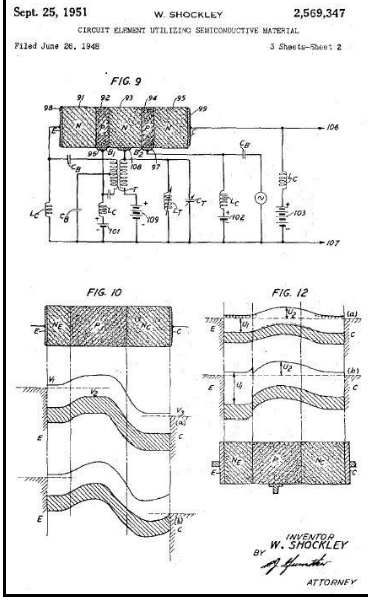
THE BIPOLAR TRANSISTOR PATENT



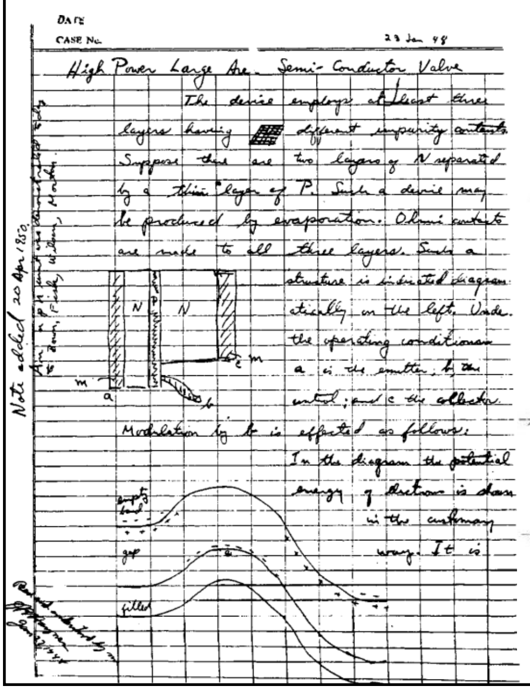
A page from the original patent by W. Shockley:

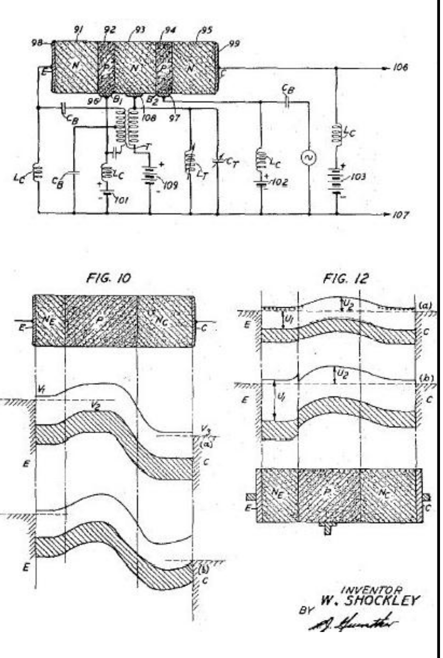
CIRCUIT ELEMENT UTILIZING SEMICONDUCTOR MATERIAL

Filed: June 26, 1948
Published: Sep 25, 1951, 2569347

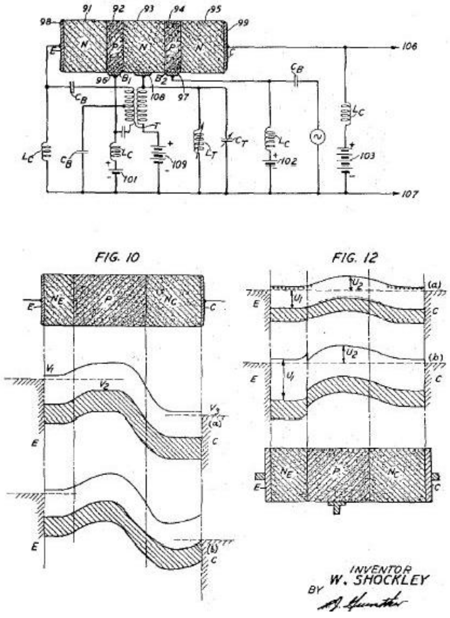
J. Bardeen, W. H. Brattain, Physical Review 74, 230 (1948)

Bardeen, *Brattain*, *Shockley*: Nobel prize in physics 1956





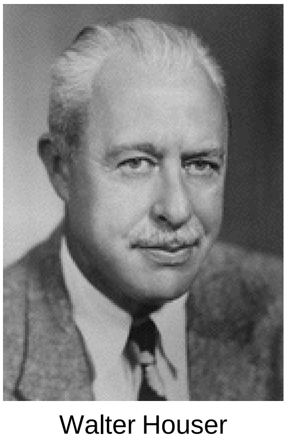
THE BIPOLAR TRANSISTOR PATENT



1947-48: THE TRANSISTOR

William Bradford Shockley (1910-1989)

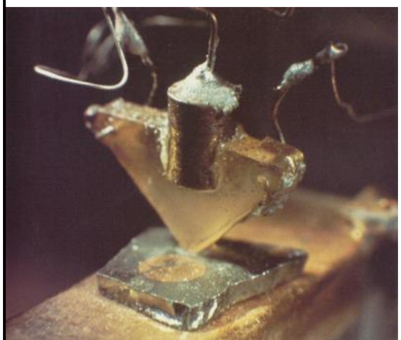
John Bardeen (1908-1991)

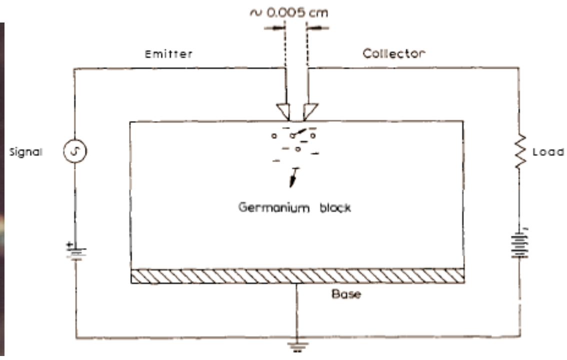


Walter Houser Brattain (1902-1987)

The Nobel Prize in Physics 1956: "for their researches on semiconductors and their discovery of the transistor effect" 50

THE POINT CONTACT TRANSISTOR: THE FIRST SEMICONDUCTOR AMPLIFIER





William Bradford SHOCKLEY, John BARDEEN, Walter Houser BRATTAIN, physics Nobel prize in1956

TRANSISTOR TRANSfer resISTOR

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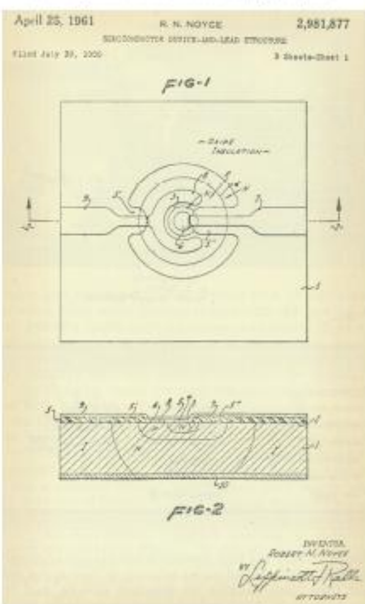
1960: THE Si IC PATENT (FAIRCHILD)



A page from the original patent by R. Noyce:

SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE

Filed: July 2?, 1960
Published: April 25, 1961, 2981877

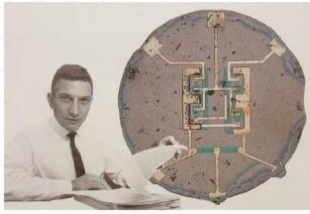
(Robert Noyce, co-founder of INTEL)

INTEGRATED CIRCUIT

First germanium and silicon integrated circuits

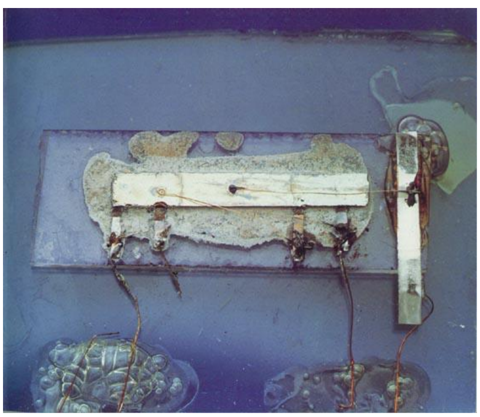
Első germánium
integrált áramkör
Jack St.Clair Kilby 1958 (TI)

Első szilicium
integrált áramkör
Robert Noice 1959 (Fairchild)



Kilby: Physics Nobel Prize 2000
The Nobel Prize in Physics 2000:
"for basic work on information and communication technology"
"for his part in the invention of the integrated circuit"

1958: INTEGRATED CIRCUIT



1958: first integrated circuit (Ge) Jack Kilby, Texas Instruments
Physics Nobel Prize 2000 (shared with Zhores I. Alferov and H. Kroemer)

THE TTL LOGIC CIRCUIT FAMILY

- Basically a modified/improved version of the diode-transistor-logic (DTL);
- Small scale integrated (SSI) circuit, short delay times;
- Input: multiemitter-transistor (AND function);
- Output: three versions, push-pull (”totem pole”), open collector, and tri-state;
- Simplest TTL logic gate: two-input NAND gate;
- Inverting gates (NAND, NOR, NOT) are easier to construct; and implement than non-inverting circuits.

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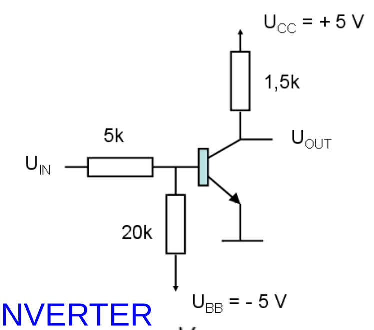
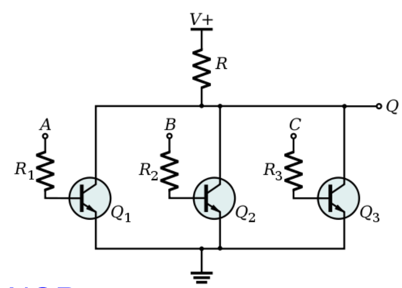
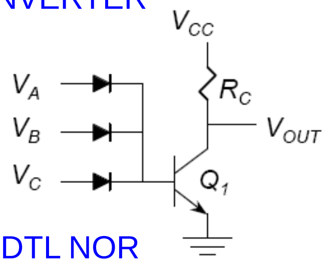
FROM SIMPLE INVERTER TO DTL GATES



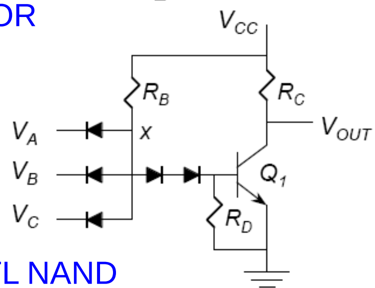
INVERTER



RTL NOR

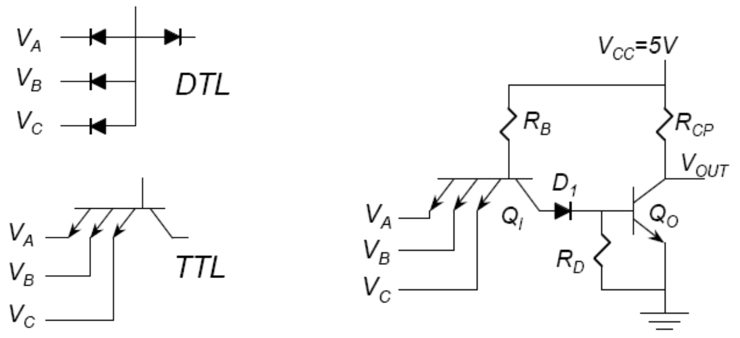


DTL NOR



DTL NAND

FROM DTL TO TTL ARCHITECTURE



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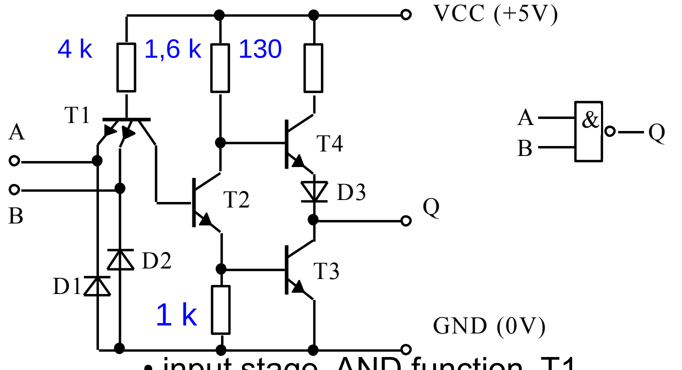
(BASIC/STANDARD) TTL GATE (NAND)



- input stage, AND function, T1,
- second stage, phase splitter, T2,
- output inverter stage with active pull-up, “totem-pole”, T3, T4, with diode level shifter, D3.
- Input diodes would be enough for the logic function, the transistor effect speeds up the switching.

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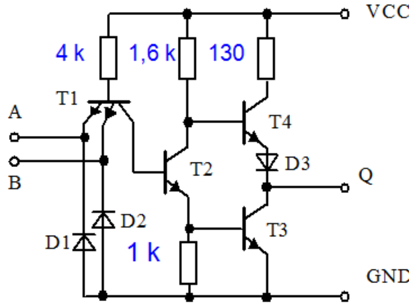
STANDARD TTL GATE (NAND)

The T4 (upper) transistor of the ”totem-pole” output is an active pull-up load, resulting in a small dynamic resistance, facilitating the fast charging up of the capacitors loading the output, and reducing the switching time.



The role of the 130 ohm resistor is the current limitation.

The multiemitter transistor was patented by Texas Instruments.

The anti-ringing diodes at the input are normally cut off. During switching transients, they turn on if an input goes more negative than -0.7V.

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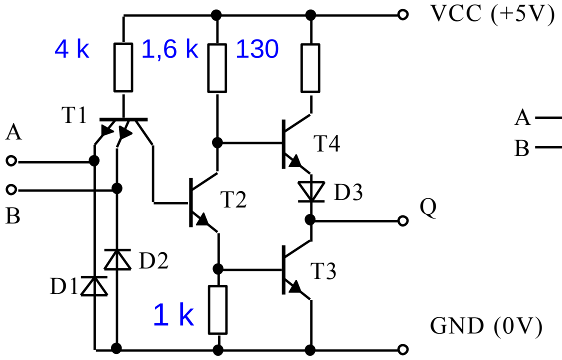
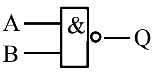
STANDARD TTL GATE BASIC OPERATION





A	B	OUT
1	1	0
X	0	1
0	X	1

NAND

If both inputs are HIGH, current through 4k and T1 BC diode (opens!) will open T2, and T3, then output goes LOW.

If any input is LOW, not enough voltage on the bases of T2 and T3, they are cut-off, output goes HIGH.

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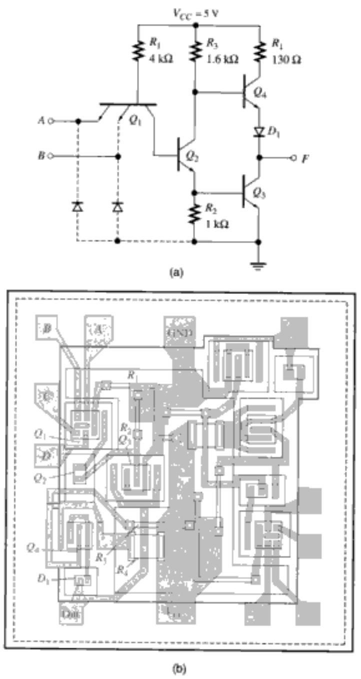
TTL NAND LAYOUT



Circuit diagram of standard 2-input TTL NAND gate

Layout of twin 4-input TTL NAND gate

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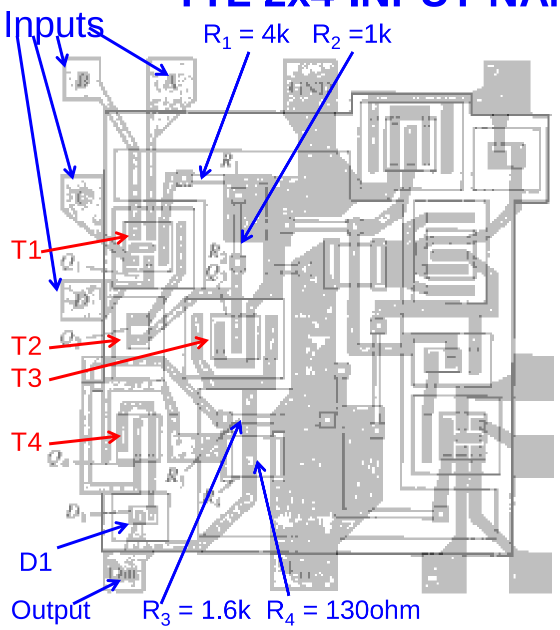
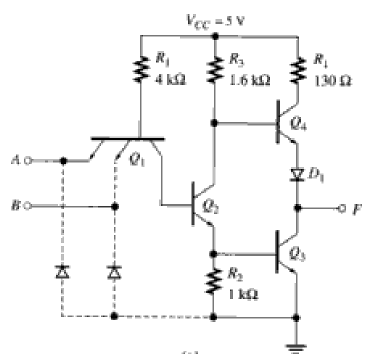
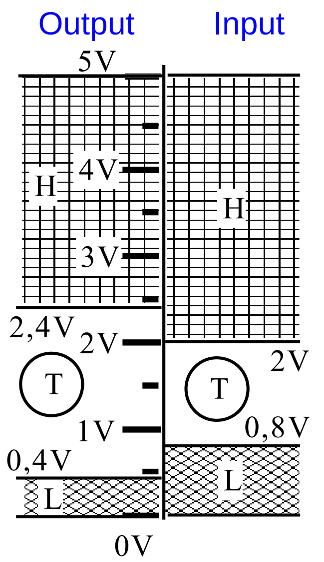
TTL 2x4-INPUT NAND GATE





TTL VOLTAGE LEVELS



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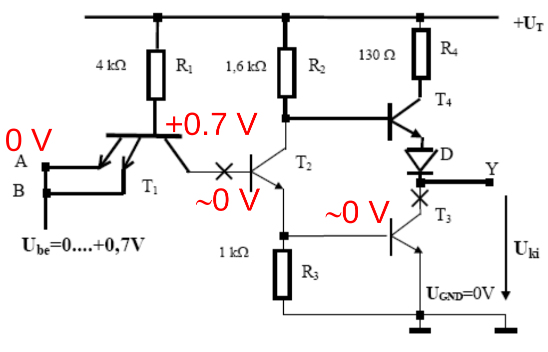
STANDARD TTL GATE VOLTAGES: INPUT LOW



T_1 és T_4 nyitott
és T_3 zárt

$U_{ki} \cong U_T - U_{BE4} - U_D \cong$
$\cong U_T - 2 \cdot U_{BE}$
+3.6 V (> +2.4 V)

$I_{in} < U_T/R_1$ = 5 V / 4 k ≈ 1,2 mA (specification: max 1.6 mA)
U_{out} (open circuit) = 5 - 2 x 0.7 = +3.6 V

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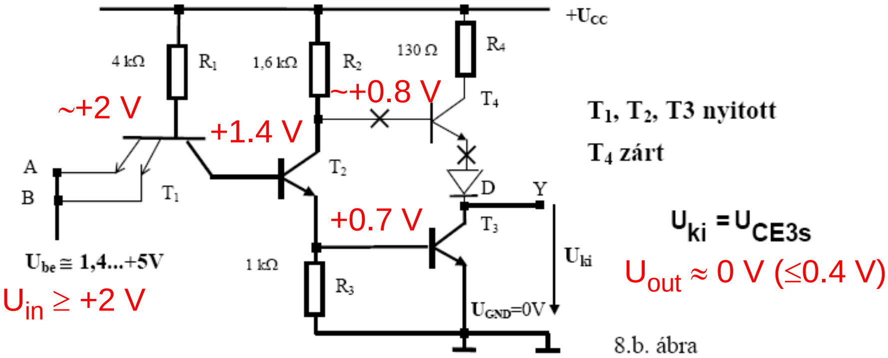
STANDARD TTL GATE VOLTAGES: INPUT HIGH



$I_{in} \le 40$ μA, $U_{out} \le 0.4$ V. T2 and T3 transistors are in saturation, this is the main speed limiting. 0 → 1 transition on output: 10-15 nsec delay. T1 and T2 transistors are in inverse mode.

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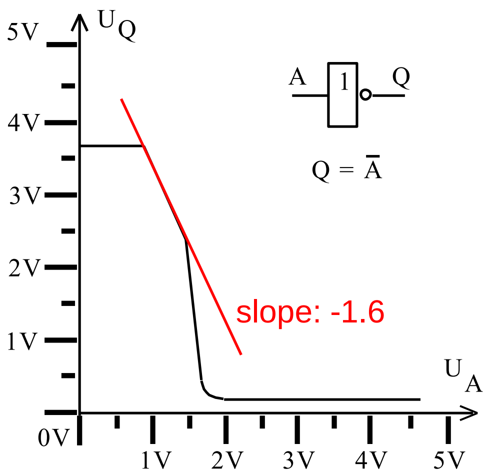
STANDARD TTL INVERTER TRANSFER CHARACTERISTICS



The shape of transfer characterisitcs is determined by the active pull-up and the totem-pole output.

In the 0.7-1.4 V input voltage region T2 transistor operates as a common emitter amplifier:

A_u = - 1.6 k / 1 k = -1.6

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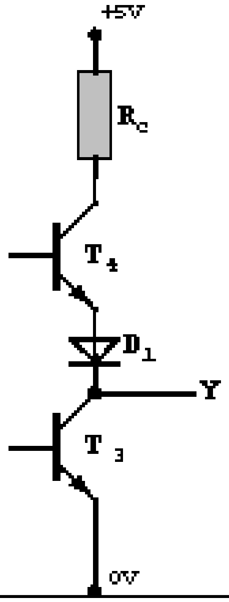
OUTPUT STAGE: TOTEM-POLE



Standard TTL circuits: push-pull output stage: ”*totem pole*”-output. This is the most common TTL output. Operation mode: pull-down and pull-up.

WARNING! TTL totem-pole outputs cannobe interconnected!

Interconnection of TTL outputs (e.g. bus system):

open collector output
tri-state output

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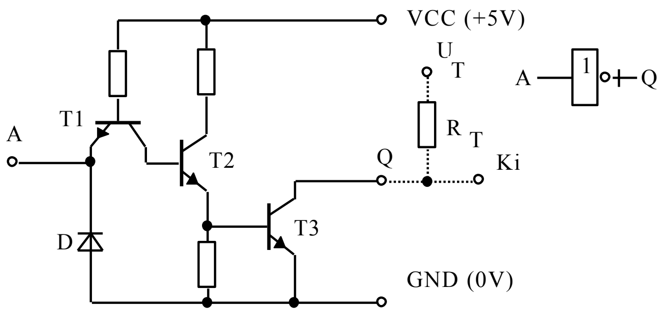
OPEN COLLECTOR OUTPUT



The output transistor is operating always in pull-down mode. If it is ON, it connects the output to ground, if it is OFF, it separates/disconnects the output (high impedance)
Applications: larger output current, larger supply voltages, etc., ”wired” logic gates.

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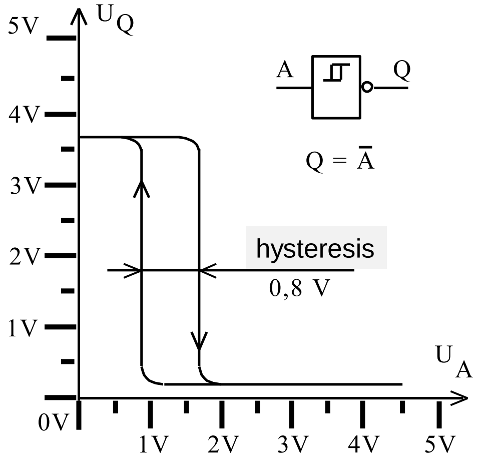
SCHMITT-TRIGGER INPUT INVERTER



Formatting input signals (speeding up).

Slowly varying, or noisy signals can be restored and processed.

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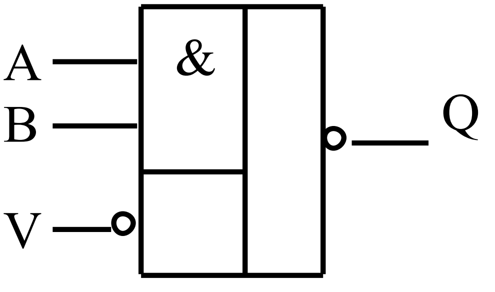
TRI-STATE OUTPUT



Input V disenables or enables the operation of the gate. If V is HIGH (disenable) the output goes to a high impedance state (toward both rail), it is *de-facto* disconnected.

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TRI-STATE OUTPUT

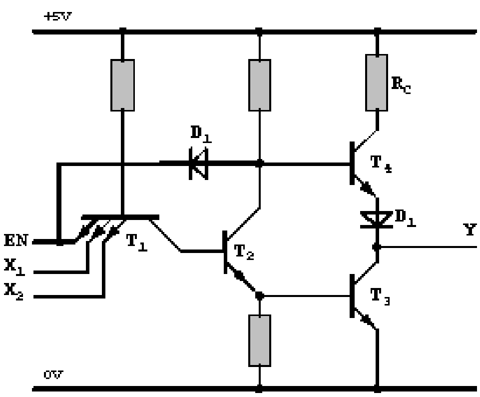
A logic device is always forcing its actual 0 or 1 level to its output. Both levels but one only at a time.

There is no such thing as three different logic level (signal), but special elements have a special state, when they are not forcing any logic signal to their output, but practically release it, if it were switched off. That is their third state.

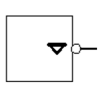
Their outputs can be parallel connected, which is prohibited in case of other gates.

TTL TRI-STATE OUTPUT

Tri-state-output: Modified version of totem-pole output. Zero level on the ENABLE input drives to cut-off both output transistor.



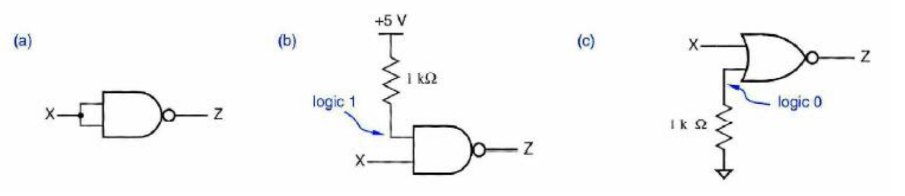
X_1	X_2	EN	Y
L	L	H	H
L	H	H	H
H	L	H	H
H	H	H	L
irrelevant		L	separated



TTL PRACTICE: UNUSED INPUTS

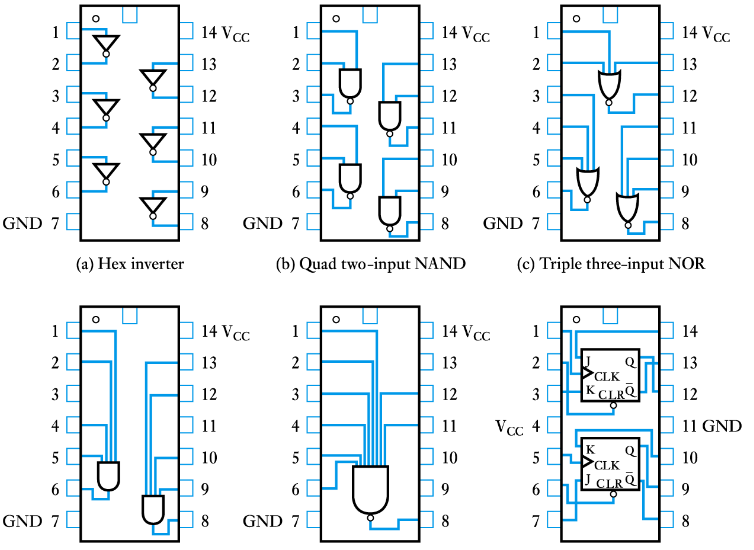
The inputs which are not used SHOULD NOT left just hanging freely! (Because of noise sensitivity).

Not used inputs should be connected to supply or ground line as appropriate through a resistor of a few kohms.



Unused inputs: (a) connected to another input, (b) NAND pulled up, (c) NOR pulled down.

TTL PRACTICE: TYPICAL PIN-OUTS



(a) Hex inverter (b) Quad two-input NAND (c) Triple three-input NOR

(d) Dual four-input AND (e) Single eight-input NAND (f) Dual J-K flip-flop

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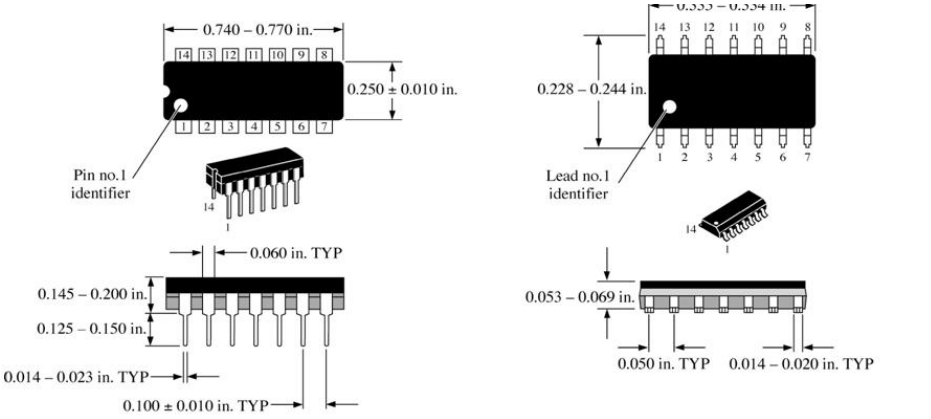
TTL PRACTICE: IC PACKAGES



(a) 14-pin dual in-line package (DIP) for feedthrough mounting

(b) 14-pin small outline package (SOIC) for surface mounting

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TTL PRACTICE: NOISE MARGINS

- Noise margin is the difference between the worst case output voltage of a stage and the worst case input voltage of the following stage.

- As larger is the noise margin, as larger is the noise voltage which when added to the signal does not cause erroneous operation.

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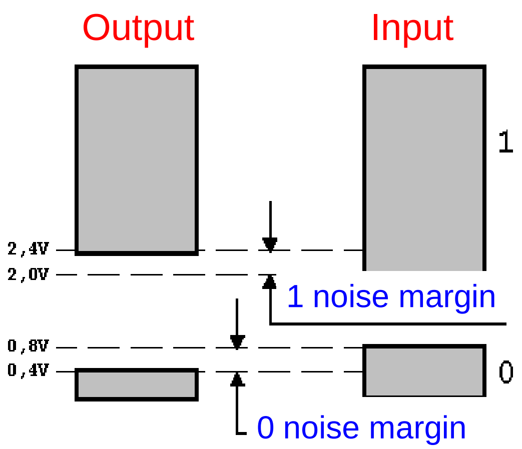
TTL STATIC NOISE MARGINS



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TTL PRACTICE: FAN-OUT

Parameter characterizing the capability of a gate output to drive several inputs simultaneously.
It is given as the number of unity loads which the gate can handle. Usually a single inverter input is the unity load.

The fan-out of standard TTL (74 series) gates is 10.

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TTL PRACTICE: POWER DISSIPATION

Static:

Ohmic losses (mostly the passive components)

Dynamic:

Ohmic losses (dissipation) during charging and discharging of the (stray) capacitances through resistors.

In standard TTL (74 series) because of the dynamic losses, at typical clock rates the dissipation is about 20 % higher than in static mode.

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POWER-DELAY PRODUCT

”Good” circuit: small delay and small power dissipation.

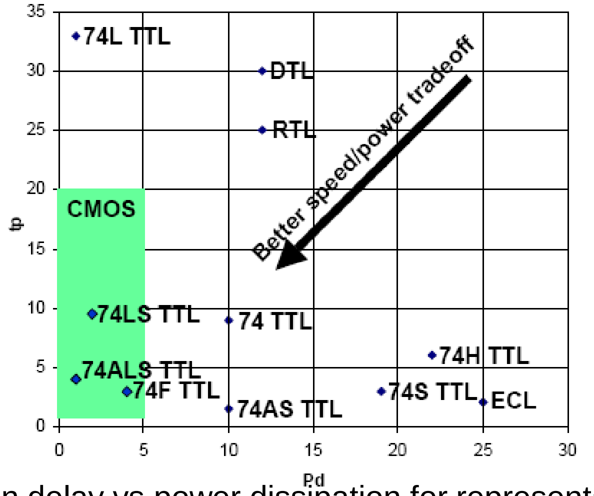
Figure-of-merit: the product of these two parameters (power-delay product).

Standard 54/74 series: t_{pd} = 10 nsec, P = 10 mW/gate

$$P\ t_{pd} = 100\ pJ$$

Interpretation: approximately the energy needed to change the value of 1 bit.

LOGIC FAMILY TRADEOFF



Propagation delay vs power dissipation for representative logic families.

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REVIEW QUESTIONS

1. What do you understand by the term logic family? What is the significance of the logic family with reference to digital integrated circuits (ICs)?

2. What is noise immunity? What is propagation delay?

3. Briefly describe propagation delay, power dissipation, speed–power product, fan-out and noise margin parameters, with particular reference to their significance as regards the suitability of the logic family for a given application.

4. What is a multiple emitter transistor?

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REVIEW QUESTIONS

5. Compare the standard TTL, low-power Schottky TTL and Schottky TTL on the basis of speed, power dissipation and fan-out capability.

6. What is the totem-pole output stage? What are its advantages?

7. What is the function of the diode at output stage of a totem pole output configuration

PROBLEMS AND EXERCISES

1. The data sheet of a quad two-input AND gate (type 74S08) specifies the propagation delay and power supply parameters as VCC =5.0V (typical), ICCH (for all four gates)=18 mA, ICCL (for all four gates)=32 mA, tpLH= 4.5 ns and tpHL =5.0 ns. Determine the speed–power product specification.

148.4 pJ

2. How many inputs of a low-power Schottky TTL NAND can be reliably driven from a single output of a Schottky TTL NAND, given the following relevant specifications for the devices of two TTL subfamilies:

Schottky TTL: IOH =1.0 mA; IIH= 0.05 mA; IOL =20.0 mA; IIL =2.0mA

Low-power Schottky TTL: IOH =0.4 mA; IIH= 0.02 mA; IOL =8.0 mA; IIL =0.4mA