DIGITAL TECHNICS II

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7. LECTURE: LOGIC CIRCUITS II: FET, MOS AND CMOS

2nd (Spring) term 2017/2018

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7. LECTURE: LOGIC CIRCUITS II: FET, MOS AND CMOS

1. The field effect transistor, FET
2. The MOS system, basic properties
3. MOSFET and basic MOS circuits
4. The CMOS concept, CMOS logic circuits

FIELD EFFECT TRANSISTOR (FET)

- Unipolar or more commonly Field Effect Transistor FET
- In a FET circuit electric field due to the input (gate-, or control electrode) voltage controls the operation of the transistor.
- As for the underlying physical mechanism the FET is a charge-controlled device.
- The output (drain-) current of a FET can be controlled with exceptionally low (practically zero) power.
- Very low power dissipation circuits (portable set-ups…).

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FET AND MOSFET

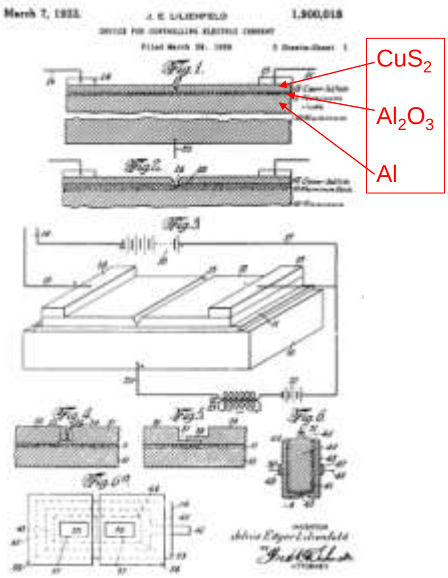
FET – Field Effect Transistor

The metal-oxide-semiconductor field-effect transistor (MOSFET) is the most important device for very-large-scale integrated circuits such as microprocessors and semiconductor memories.

Voltage applied to insulated gate controls current between source and drain. Low power allows very high integration.

The principle of the surface field-effect transistor was first proposed in the 1930s by Lilienfeld (US patent) and Heil (British patent).

THE FET PATENT



A page from the original patent by J. Lilienfeld

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Filed: March 28, 1928
Published: March 7, 1933
1900018

In today's concepts:
Depletion type p-channel MOSFET

J. LILIENFELD AND THE FET

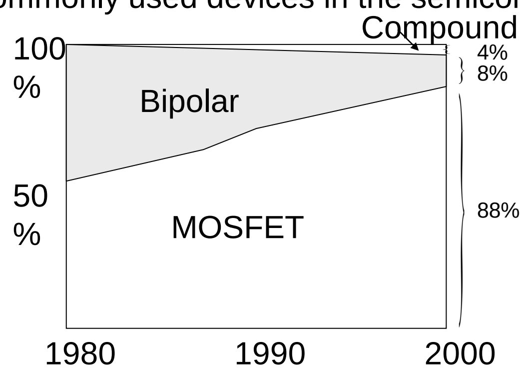
Julius Edgar Lilienfeld (1882-1963) was an Austro-Hungarian physicist. He was born in Lemberg, Galicia, in Austria-Hungary (now called Lviv in Ukraine), moved to the United States in the early 1920s.

Lilienfeld is credited with the first patents on the field effect transistor (1920s) and electrolytic capacitor (1931).

He filed several patents describing the construction and operation of transistors as well as many features of modern transistors. (US patent #1,745,175 for an FET-like transistor was granted January 28, 1930.) When Brattain, Bardeen, and Robert Gidney tried to get patents on their earliest devices, most of their claims were rejected due to the Lilienfeld patents.

MOS TRANSISTOR: RELEVANCE

- Metal-oxide-semiconductor
- Also called MOSFET (MOS Field Effect Transistor)
- Simple, symmetric structure
- Switch, good for digital, logic circuit
- Most commonly used devices in the semiconductor industry



Market of semiconductor products

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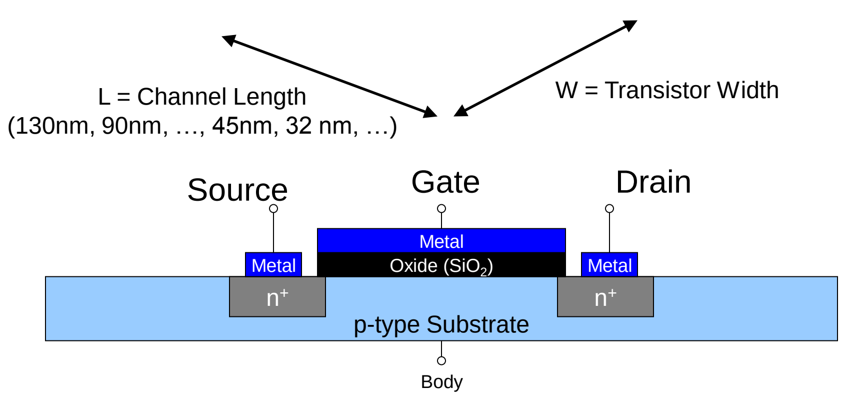
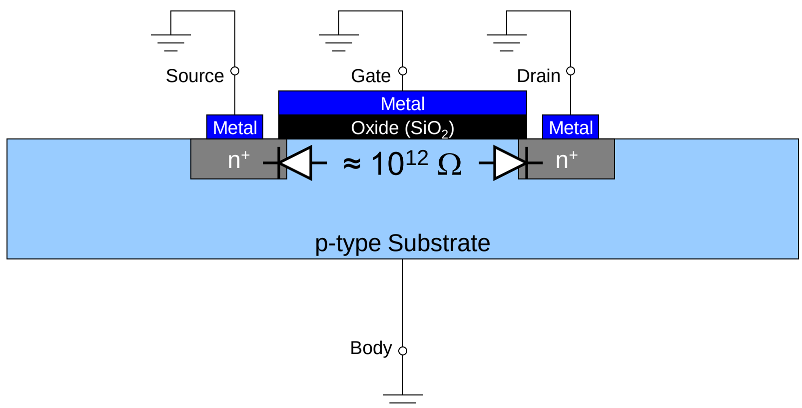
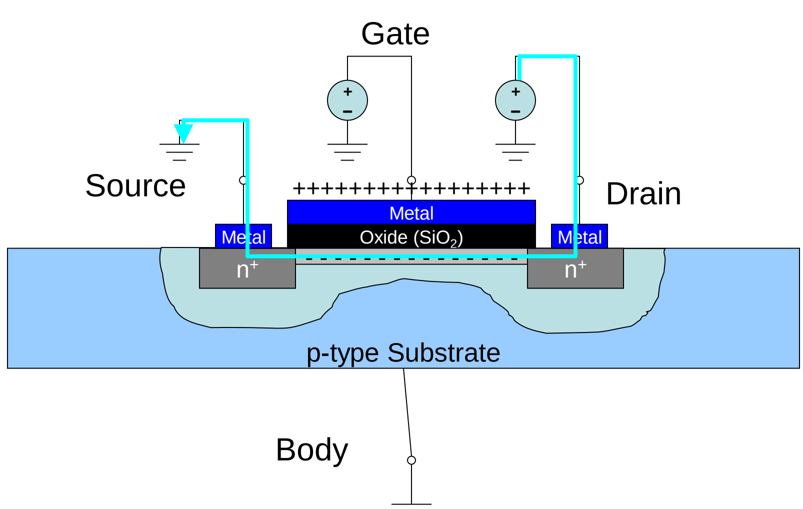
NMOS TRANSISTOR



NMOS $U_{gate} = 0$



NMOS $U_{gate} > 0$, $U_{ds} > 0$



Voltage-controlled resistance: increase $U_{gate} \Rightarrow$ decrease R_{DS}

THRESHOLD VOLTAGE

Increasing U_{gate} depleats the layer below the gate (the hole concentration decreases gradually),

Reaching a the *threshold voltage* (U_T), an opposite type, i.e. n-type conducting channel is formed (*inversion layer)*.

The threshold voltage U_T depends on
- Dopant concentration (technological control !)
- Substrate bias
- Temperature

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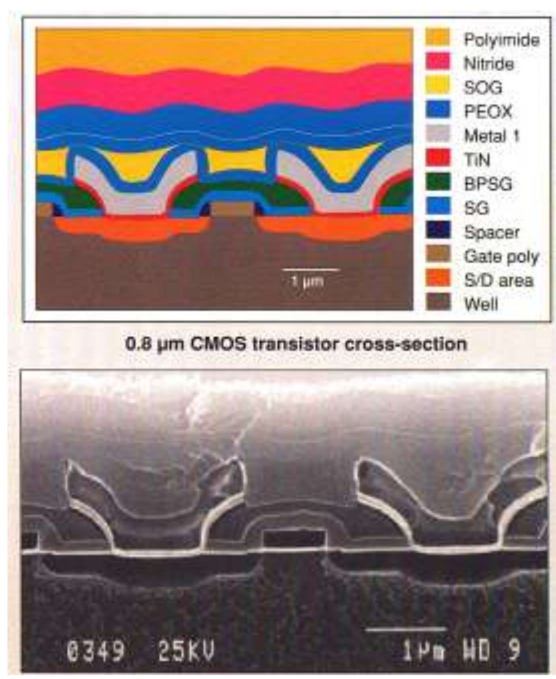
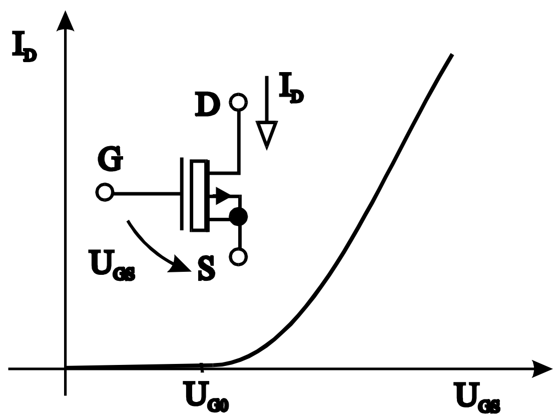
MOS TRANSISTOR

Sub-micrometre MOSFET structure

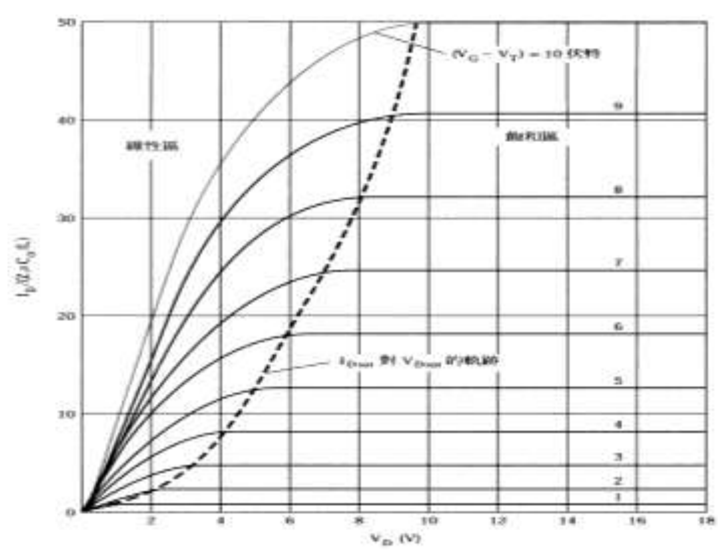
Schematic cross-section and SEM picture



DRAIN CURRENT-GATE VOLTAGE CHARACTERISTICS OF MOSFET



MOSFET OUTPUT CHARACTERISTICS



MOS CHARACTERISTICS

The analytic form of the input (transfer) characteristics based on the elementary physical model is

$$I_{DS} = K\,(U_{GS} - U_T)^2$$

K – device constant (depends on the technology and geometry of the device

U_T- turn on or threshold voltage

The current through the device is

$$I_{DS} = K((U_{GS} - U_T) - U_{DS}/2)U_{DS}$$

MOSFET AS A SWITCH

The MOSFET can be considered in a very good approximation as an ideal switch.

When closed (cut-off) the resistance is greater than 10^{10}-10^{12} ohm.

When open the resistance is a few hundred ohms, this can be taken as a short circuit with respect to the cut-off state.

The switchover can be controlled practically without power.

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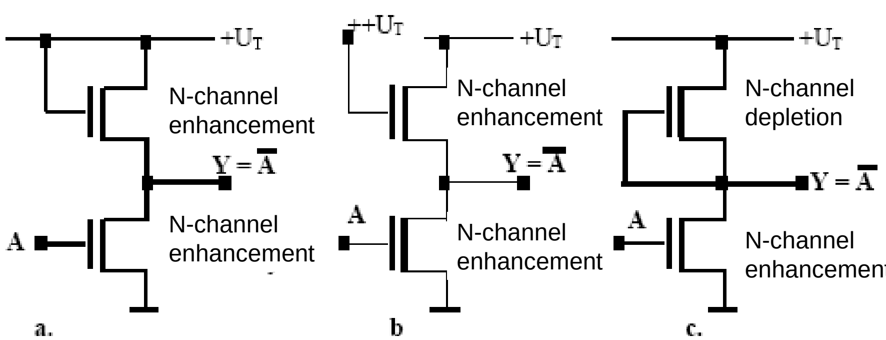
MOS CIRCUITS AND LOGIC GATES: BASIC PRINCIPLES

Basic circuit: inverter, both the control- (driver-) transistor and the load are active elements.

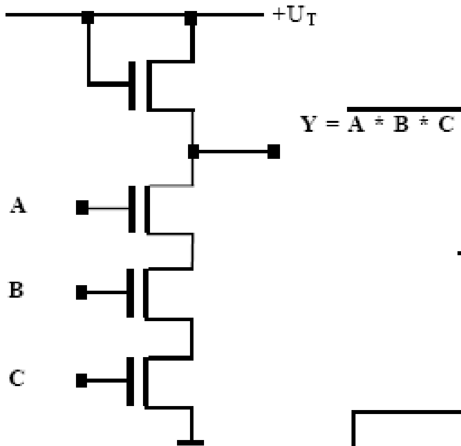
Inverter with passive loading: the load transistor is not controlled by the input. Its gate is connected to the supply voltage or to an other electrode of the transistor.

Inverter with active load: the loading transistor is also controlled by the input signal. In this case one of the transistors is of NMOS, the other is of PMOS type.

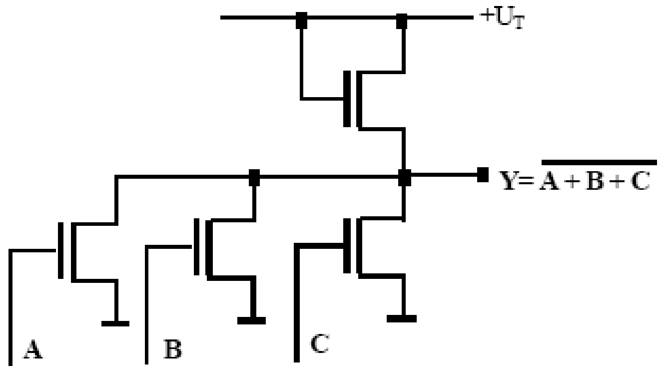
NMOS INVERTER BASIC CIRCUITS WITH PASSIVE LOADING



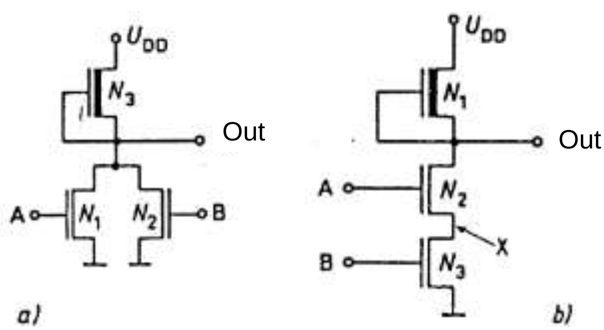
BASIC MOS CIRCUITS: NOR & NAND GATE



MOS circuits are simple. The control- (drive-) transistors determine the logic function. Even in the case of complex logic functions, one load transistor is sufficient.



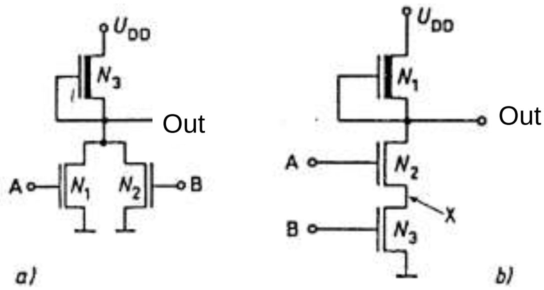
NMOS GATES: NOR AND NAND



2-input NOR (a) and NAND (b) gates

NOR gate: the dimensions (length and width) of the driver gates are the same as in the inverter. If only one of them is open, the output LOW level and the time is also the same. If both driver inputs are HIGH, both parallel transistors will be open, and the above parameters will be improved.

NMOS GATES: NOR AND NAND



2-input NOR (a) and NAND (b) gates

NAND gate: For N inputs, the widths (W) of the driver transistors are N times wider, to ensure the same output LOW level and time as in the case of the inverter.
Usually at most four transistors are connected in series, because the too large dimensions result in too large capacitive loads, which will increase the propagation delay of the circuit.

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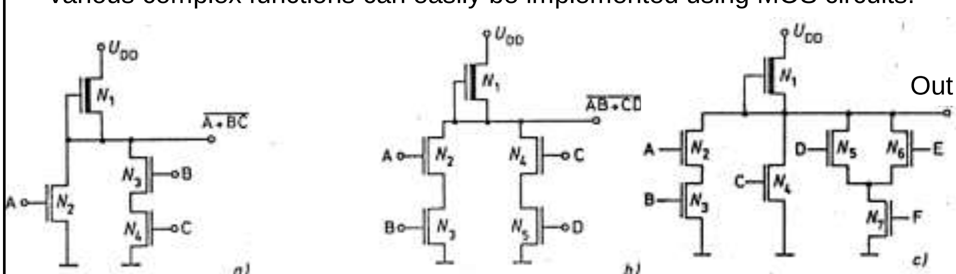
COMPLEX GATES

Various complex functions can easily be implemented using MOS circuits:



$\overline{AB+C+(D+E)F}$

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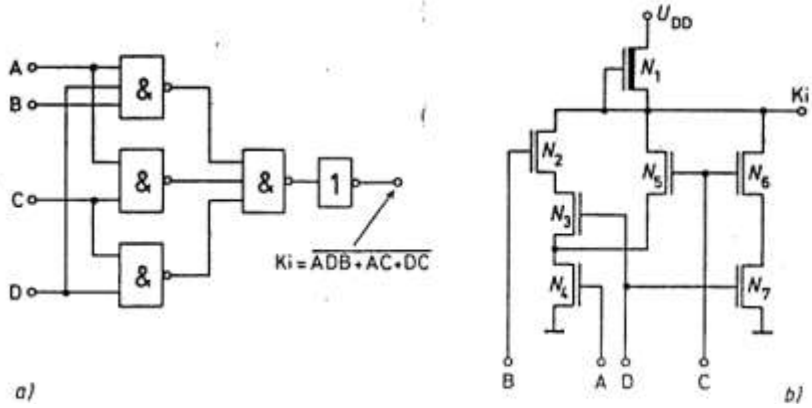
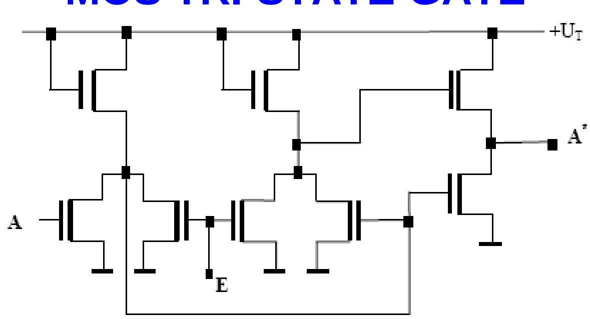
COMPLEX GATES



The feasibility of complex gates offers new possibilities with respect to customary TTL circuit solutions. E.g. the TTL circuit consisting of five gates (a) can be implemented with a 7-transistor complex gate (b).
Advantages: (i) fewer components, (ii) faster operation (the complex gate is only one gate with one unit delay), while the (a) version represents 3 units of delay.

MOS TRI-STATE GATE



- E = 1 closes both output transistor (drives them to high impedance state). The output is separated from the next stage.
- E = 0 then A* = A.

In fact there is no third logic level or state.
In its „third” state it does nor impress any logic level to its output. Just allows its output level to be determined by an output of an other gate on the same bus line.

THE MOSFET AND CMOS INTEGRATED CIRCUITS

The Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) is the prevailing device in microprocessors and memory circuits.

The MOSFET's advantages over other types of devices are its (i) mature fabrication technology, (ii) its successful scaling characteristics and (iii) complementary MOSFETs yielding CMOS circuits.

The fabrication process of silicon devices has evolved over the last 40 years into a mature, reproducible and reliable integrated circuit manufacturing technology.

CMOS LOGIC CIRCUITS

CMOS technology uses both NMOS and PMOS transistors. The transistors are arranged in a structure formed by two complementary networks:

pull-up network is complement of pull-down;
parallel→series, series→parallel.

CMOS logic circuits may be considered switching circuits because of the extreme little control current necessary.

Most commonly used circuit in IC chip since 1980s.

Low power consumption.
High temperature stability.
High noise immunity.
Symmetric design.
Still dominates the IC market.
Backbone of information revolution.

HISTORICAL OVERVIEW

MOS ⇒ metal oxide semiconductor
IG ⇒ insulated gate
MIS ⇒ metal insulator semiconductor

History of MOS (more generally FET) devices

Early 1930s ⇒ Principle of the surface field-effect transistors was proposed and patented by *Julius Lilienfield* and *Oscar Heil*.

Late 1940s ⇒ The future Nobelist *Shockley* and *Pearson* of AT&T Bell Labs studied the theory of MOS (FET) devices.

1960 ⇒ *Kahng* and Atalla of Bell Labs fabricated the first MOSFET using a thermally oxidized silicon structure.

1962 ⇒ *Weimer* of RCA filed a US patent on a CMOS flip flop.

1963 ⇒ *Wanlass* of Fairchild filed a US patent on a CMOS inverter, NOR, and NAND gates.

1970 ⇒ Processes using nMOS became dominant.

1980 ⇒ Power consumption become a major issue. CMOS process are widely adopted.

Note: In conventional CMOS, only enhancement mode (normally off) MOSFETs are used. We do not use depletion mode (normally on) device.

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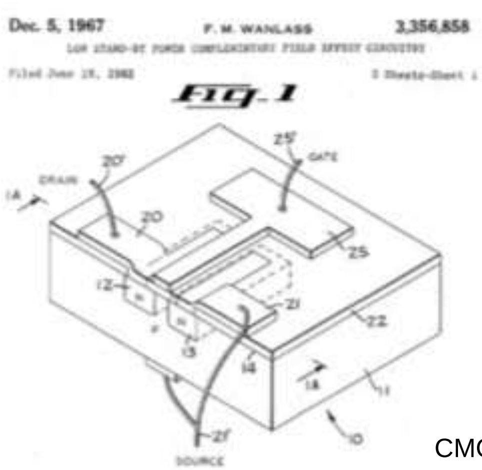
1963: COMPLEMENTARY MOS CONFIGURATION IS INVEVTED



In a 1963 conference paper C. T. Sah and Frank Wanlass of the Fairchild R & D Laboratory showed that logic circuits combining p-channel and n-channel MOS transistors in a complementary symmetry circuit configuration drew close to zero power in standby mode. Wanlass patented the idea that today is called CMOS.

CMOS device structure from Frank Wanlass's patent drawing

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TECHNOLOGY SCALING

1971: Intel 4004
transistors with minimum dimension of 10um

2003: Pentium 4
transistors with minimum dimension of 130 nm

200x: Intel 45nm node (high-k gate stack, stressed Si…)

2016 and beyond: Scaling cannot go on forever because transistors cannot be smaller than atoms …

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POWER SUPPLY VOLTAGE

GND = 0 V

In 1980's, V_{DD} = 5V

V_{DD} has decreased in modern processes

High V_{DD} would damage modern tiny transistors

Lower V_{DD} saves power

V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, …

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CMOS LOGIC FAMILIES

The CMOS (Complementary Metal Oxide Semiconductor) logic family uses both N-type and P-type MOSFETs (enhancement MOSFETs, to be more precise) to realize different logic functions. The two types of MOSFET are designed to have matching characteristics. That is, they exhibit identical characteristics in switch-OFF and switch-ON conditions.

The main advantage of the CMOS logic family over bipolar logic families lies in its extremely low power dissipation, which is near-zero in static conditions. In fact, CMOS devices draw power only when they are switching. This allows integration of a much larger number of CMOS gates on a chip than would have been possible with bipolar or NMOS technology. CMOS technology today is the dominant semiconductor technology used for making microprocessors, memory devices and application-specific integrated circuits (ASICs).

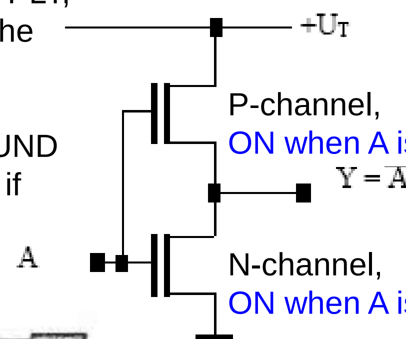
CMOS LOGIC FAMILY

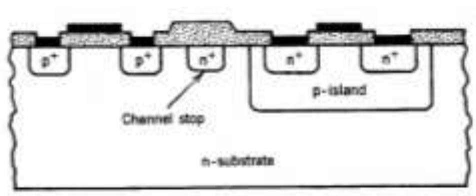
The CMOS logic family, like TTL, has a large number of subfamilies. The basic difference between different CMOS logic subfamilies such as 4000A, 4000B, 4000UB, 74C, 74HC, 74HCT, 74AC and 74ACT is in the fabrication process used and not in the design of the circuits employed to implement the intended logic function.

BASIC CMOS CIRCUIT: THE INVERTER

PMOS connected to + SUPPLY, pulls up the output level if the input is 0.

NMOS connected to GROUND pulls down the output level if the input is 1.

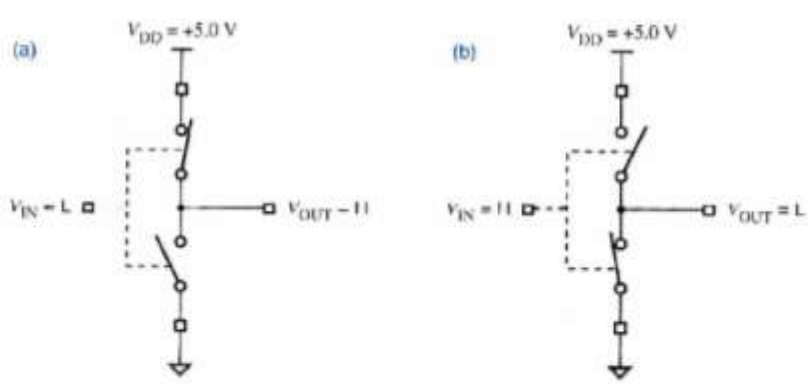




CMOS inverter:

nMOS/pMOS transistor pair

CMOS INVERTER AS A SWITCHING CIRCUIT



Switch model of a CMOS inverter. a. input LOW, b. input HIGH.

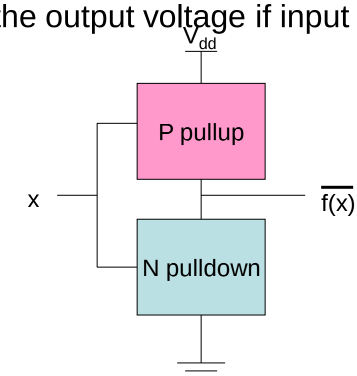
COMPLEMENTERY MOS: CMOS

n-channel and p-channnel MOS transistor pairs

PMOS

drain connected to high (+) supply voltage

pulls-up the output voltage if input is 0 (low).



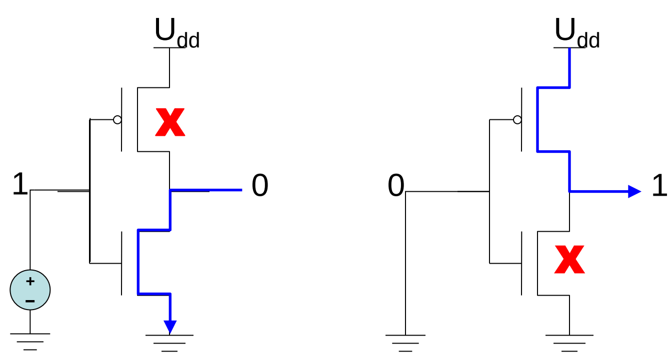
NMOS

source connected to zero supply voltage (GND)

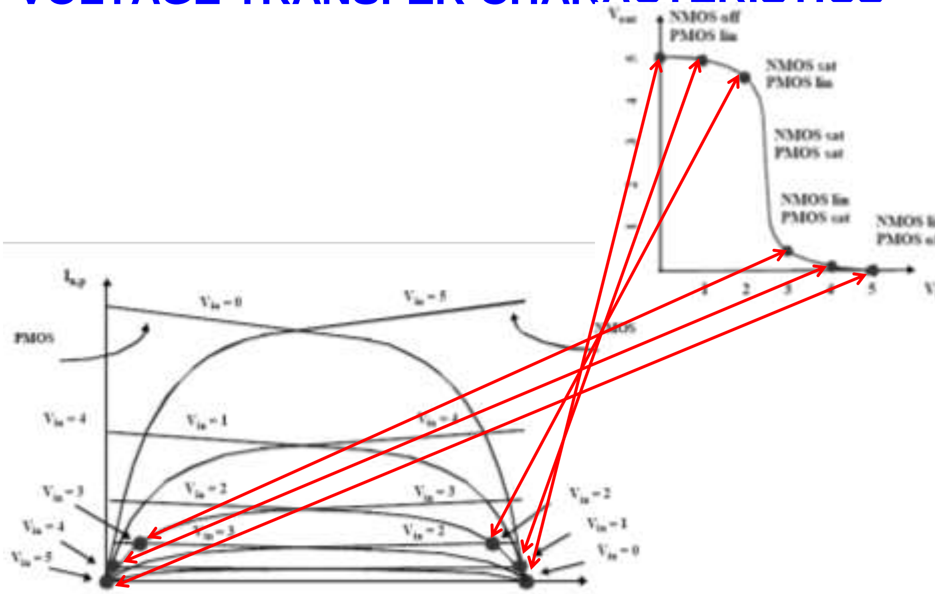
pulls-down the output voltage if input is 1 (high).

CMOS INVERTER

- If input is 1, output is 0
- If input is 0, output is 1



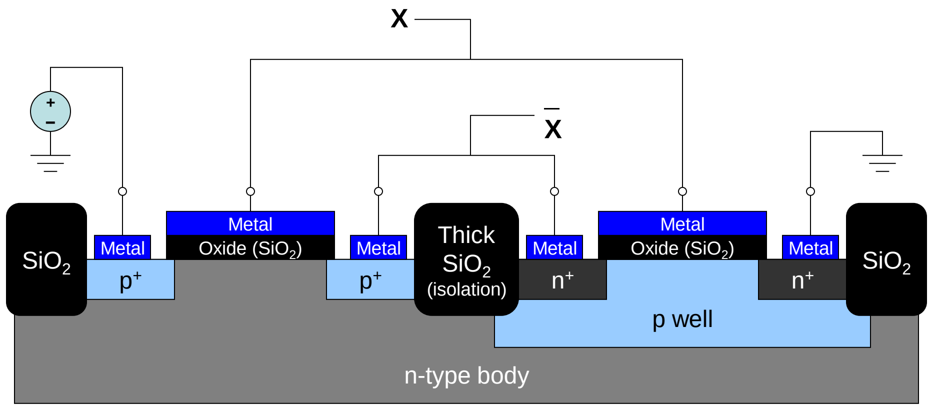
CMOS INVERTER LOAD AND VOLTAGE TRANSFER CHARACTERISTICS



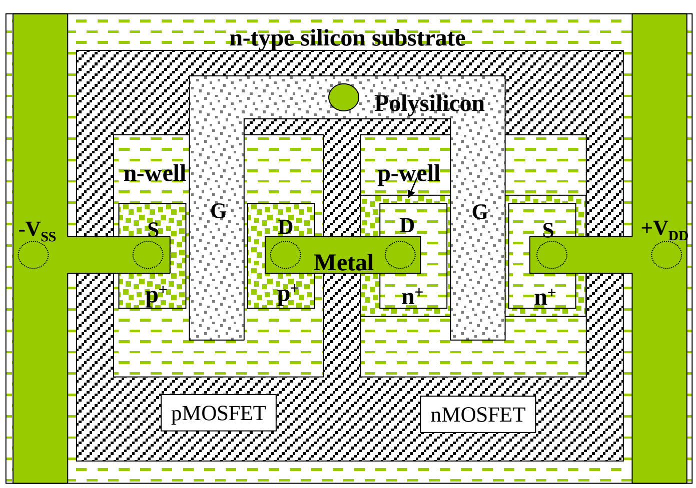
CMOS LOGIC CITCUITS: MAIN FEATURES

- MOSFET occupies the smallest area on the Si wafer
- MOSFET can be fabricated with less number of steps
- MOSFET is controlled with practically zero power
- In stationary state it does not draw current from the supply
- Supply voltage can vary in a wide range
- No resistors are necessary

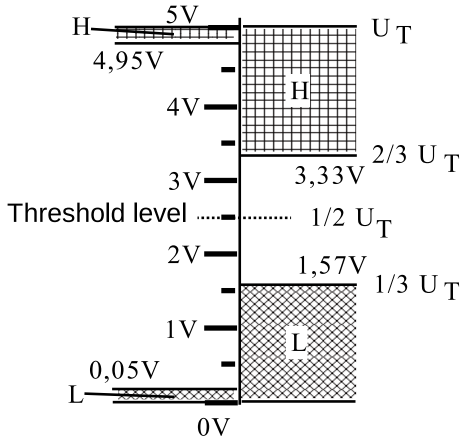
TECHNOLOGICAL IMPLEMENTATION OF CMOS INVERTER



TOP VIEW OF A CMOS INVERTER



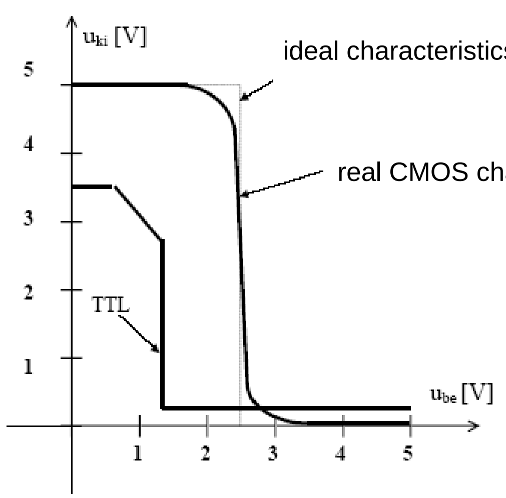
CMOS LOGIC VOLTAGE LEVELS (SSI MODULAR LOGIC)



CMOS logic voltage levels with +5 V supply voltage.

Can operate with supply from +3 to +15 V.

(SSI MODULAR) CMOS INVERTER: TRANSFER CHARACTERISTICS



POWER DISSIPATION

The dynamic dissipation increases linearly with increase in clock frequency - we will investigate the reason for this later in the course.

$$P_{dynamic} = f\, C\, V_{DD}^2$$

The control of capacitance is also important.

CMOS ENERGY AND POWER EQUATIONS

$$E = C_L\, V_{DD}^2\, P_{0\to1} + t_{sc}\, V_{DD}\, I_{peak}\, P_{0/1\to1/0} + V_{DD}\, I_{leak}$$

$$f = P * f_{clock}$$

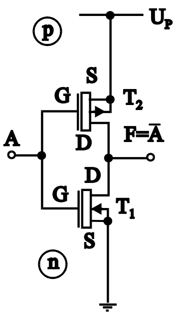
$$P = C_L\, V_{DD}^2\, f + t_{sc} V_{DD}\, I_{peak}\, f + V_{DD}\, I_{leak}$$

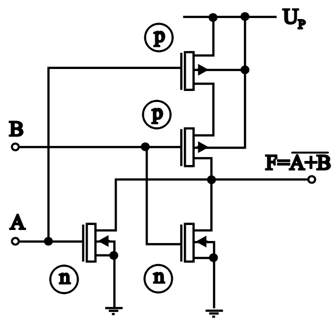
Dynamic power (~80% today and decreasing relatively)

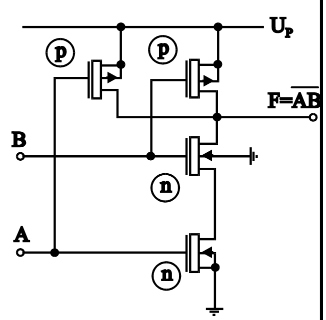
Short-circuit power (~5% today and decreasing absolutely)

Leakage power (~15% today and increasing)

BASIC CMOS GATES

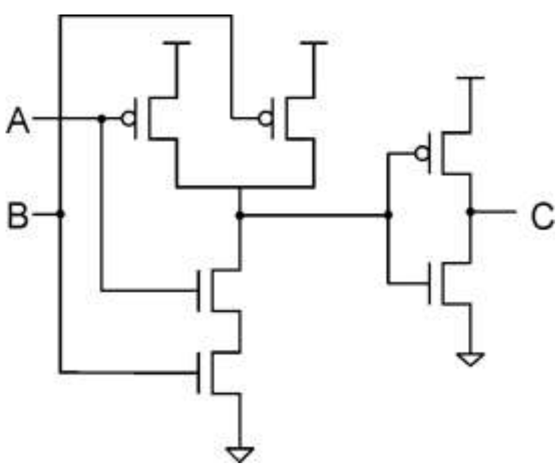






INVERTER NOT-OR (NOR) NOT-AND (NAND)

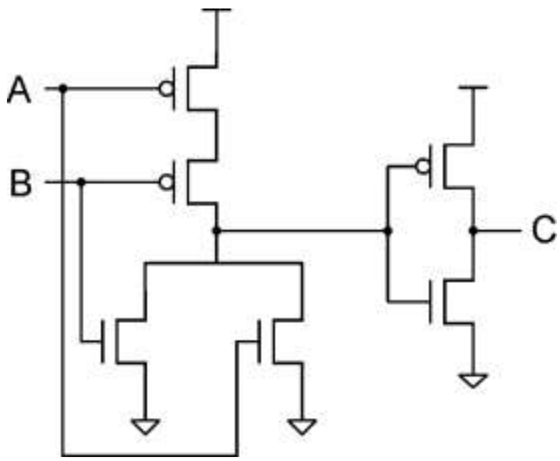
AND GATE



A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Add inverter to NAND.

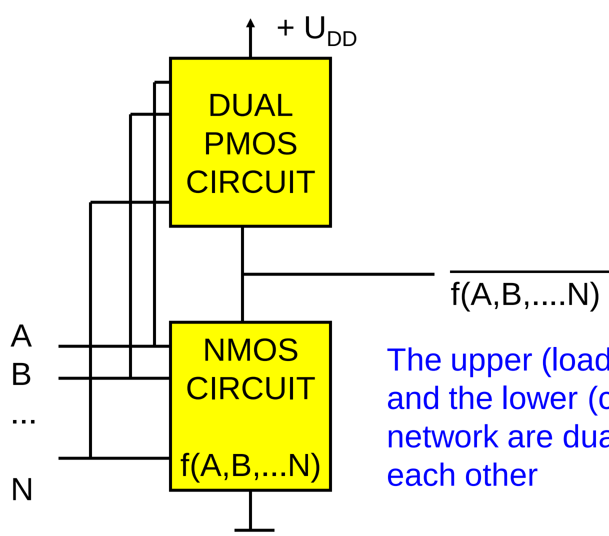
OR GATE



A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

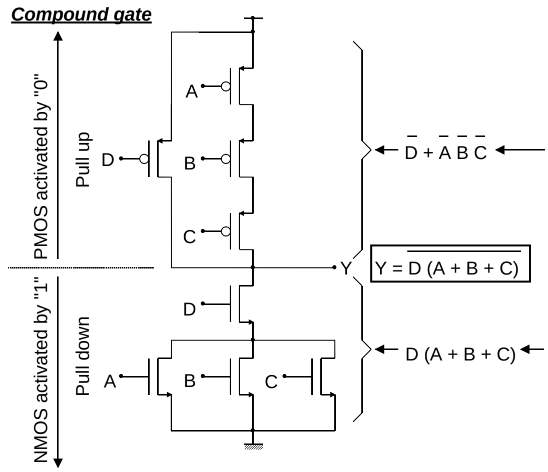
Add inverter to NOR.

CMOS COMPLEX GATES: GENERAL PRINCIPLE



The upper (load) network and the lower (control) network are duals of each other

DESIGNING CMOS GATES



Y	AB 00	01	11	10
CD 00	1	1	1	1
01	1	0	0	0
11	0	0	0	0
10	1	1	1	1

Y	AB 00	01	11	10
CD 00	1	1	1	1
01	1	0	0	0
11	0	0	0	0
10	1	1	1	1

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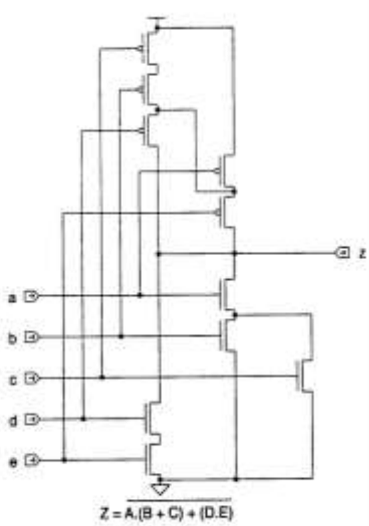
CMOS COMPLEX GATE



Each logic function is duplicated for both pull-down and pull-up logic tree

- pull-down tree gives the zero entries of the truth table, i.e. implements the negative of the given function Z
- pull-up tree is the dual of the pull-down tree, i.e. implements the true logic with each input negative-going

Advantages: low power, high noise margins, design ease, functionality

Disadvantage: high input capacitance reduces the ultimate performance

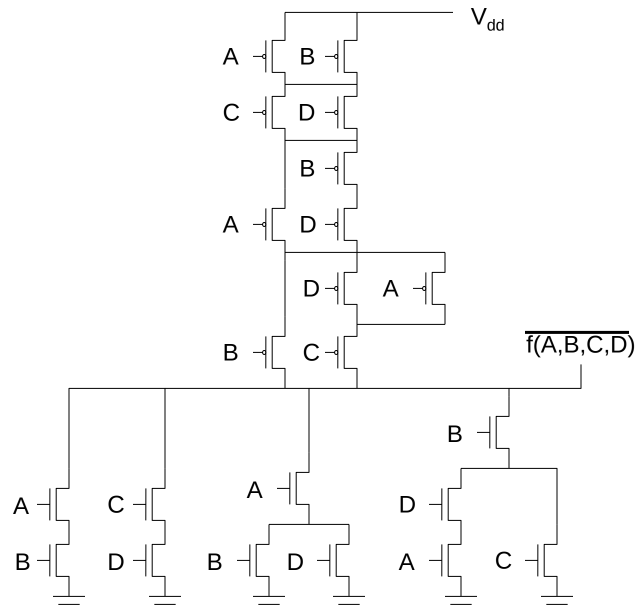
EXAMPLE OF A COMPLEX GATE

Complement
for PMOS=

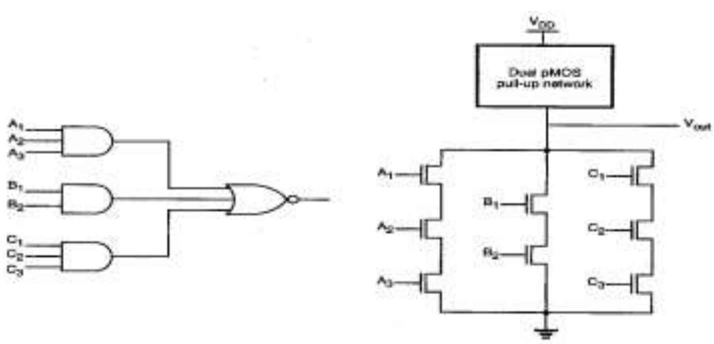
(A+B)
. (C+D)
. (A+(B.D))
. (B+((D+A).C))

f(A,B,C,D) =

A.B
+ C.D
+ A.(B+D)
+ B.(D.A+C)

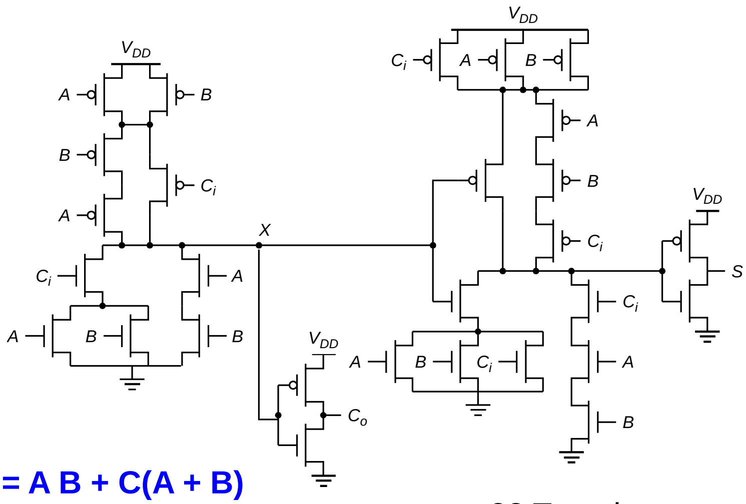


AOI (AND-OR-INVERT) CMOS GATE



AOI complex CMOS gate can be used to directly implement a sum-of-products Boolean function
The pull-down N-tree can be implemented as follows:
Product terms yield series-connected NMOS transistors
Sums are denoted by parallel-connected legs
The complete function must be an inverted representation
The pull-up P-tree is derived as the dual of the N-tree

STATIC CMOS FULL ADDER



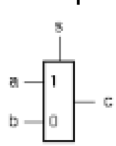
C_{out} = A B + C(A + B)

28 Transistors

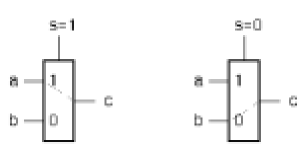
$S = (A + B + C)\overline{C_{out}} + A\,B\,C$

TRANSISTOR-LEVEL LOGIC CIRCUITS: MUX

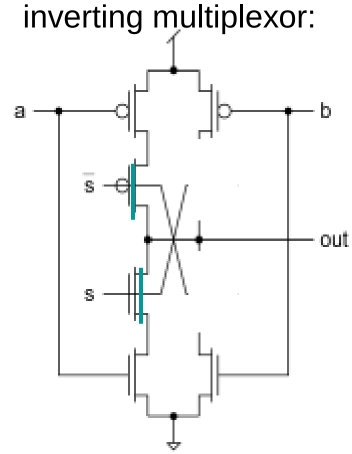
- Multiplexor



If s=1 then c=a else c=b



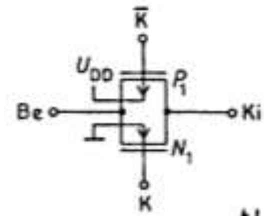
- Transistor Circuit for inverting multiplexor:



TRANSFER GATE

Transmission gates are the way to build “switches” in CMOS.

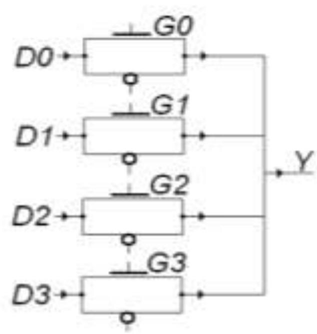
Both transistor types are needed:
nFET to pass zeros.
pFET to pass ones.



Architecture: nFET and pFET connected in parallel, gates driven in opposite phase.
The transmission gate is bi-directional (unlike logic gates and tri-state buffers).
Functionally it is similar to the tri-state buffer, but does not connect to V_{dd} and GND, so must be combined with logic gates or buffers.

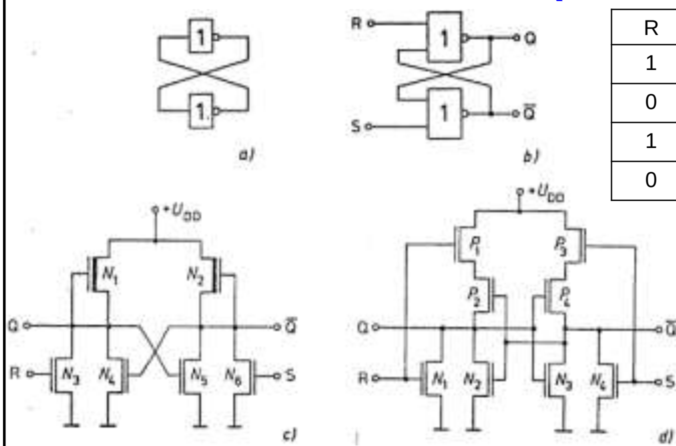
Using transfer gates significant circuit simplifications can be realized.

MULTIPLEXERS IN CMOS



4-to-1 multiplexer implemented with CMOS transfer gates.
Very transistor efficient solution!

RS FLIP-FLOP (LATCH)



R	S	Q	Q(-)
1	1	0*	0*
0	1	1	0
1	0	0	1
0	0	Q**	Q(-)**

* forbidden state
** holding state

a) bistability principle, b) RS flip-flop (latch), c) depletion MOS load implementation, d) CMOS implementation

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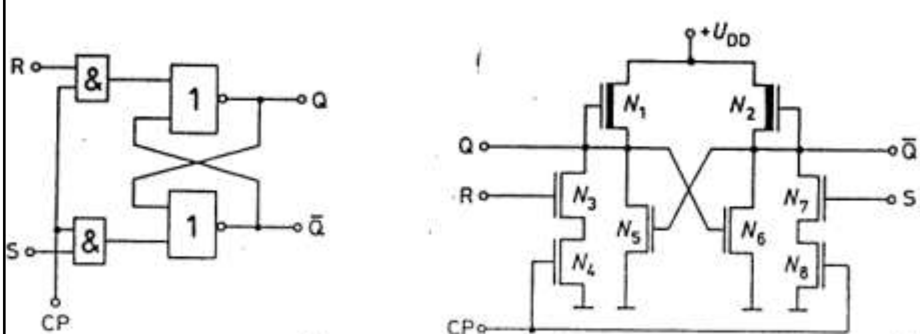
CLOCK CONTROLLED RS FLIP-FLOP



Logic diagram and NMOS implementation

Note the simplification achieves by realizing the series connected AND and NAND gates with a complex gate.

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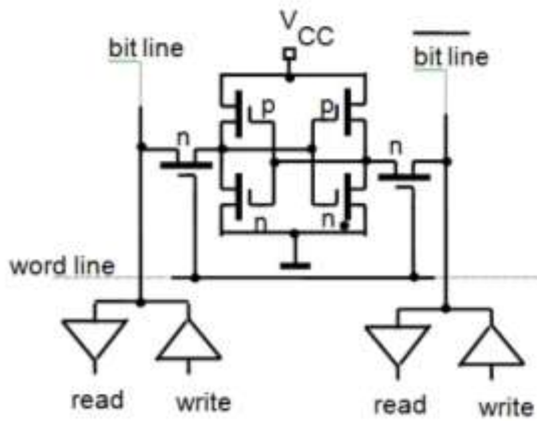
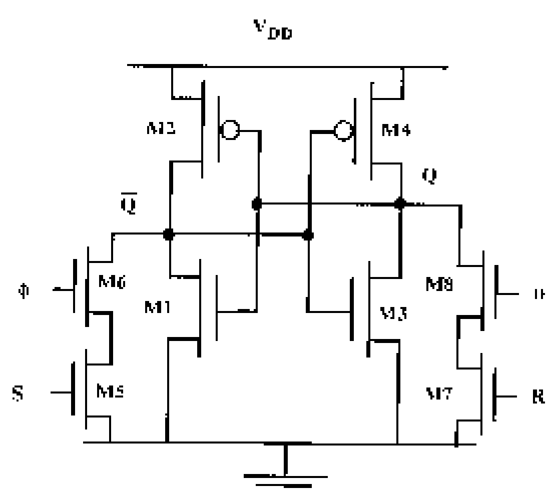
CMOS STATIC RAM CELL

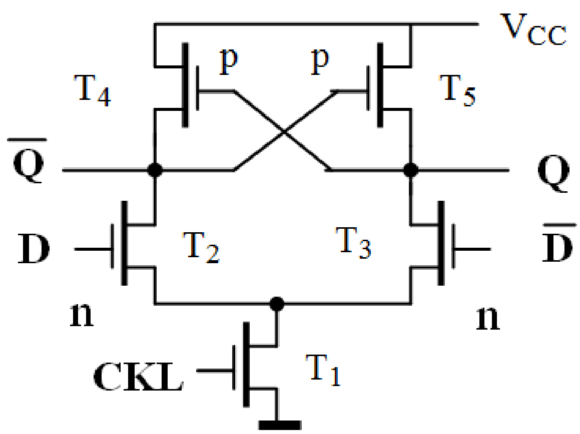


Six-transistor CMOS RAM memory cell: two cross-coupled CMOS inverters (RS flip-flop). R/W through two nMOS transistors

CMOS CLOCKED SR FLIP-FLOP



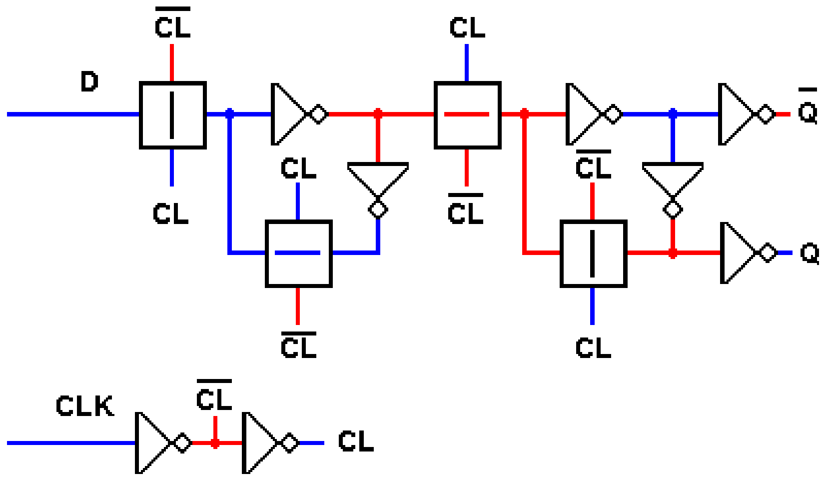
CLOCKED CMOS D FLIP-FLOP



CMOS D FLIP-FLOP

- CMOS technology allows a very different approach to flip-flop design and construction. Instead of using logic gates to connect the clock signal to the master and slave sections of the flip-flop, a CMOS flip-flop uses *transmission gates* to control the data connections.

CMOS D FLIP-FLOP SCHEMATIC



LOGIC FAMILY CHARACTERISTICS

- **Complementary metal oxide semiconductor (CMOS)**
  - most widely used family for large-scale devices
  - combines high speed with low power consumption
  - in the past operated from a single supply of 5 – 15 V
  - excellent noise immunity of about 30% of supply voltage
  - can be connected to a large number of gates (about 50)
  - many forms – some with t_{PD} down to 1 ns
  - power consumption depends on speed (perhaps 1 mW)
  - V_{DD} has decreased in modern processes, high V_{DD} would damage modern tiny transistors, lover V_{DD} saves power
  - V_{DD} = 3.3, 2,5, 1.8, 1,5, 1.2, 1,0, …

CMOS LOGIC FAMILIES

C	- 4-15 V operation (similar to 4000 series)
HC	- High speed, similar performance to LS
HCT	- high speed, compatible logic levels to bipolar parts
AC	- Advanced, performance generally between S and F
AHC	- Advanced high speed, 3x faster than HC
FC	- Fast, performance similar to F
LCX	- 3V supply and 5 volt tolerant inputs
LVQ	- Low voltage 3.3 V
LVX	- Low voltage 3.3 V with 5 V tolerant inputs
VHC	- very high speed „S” performance in CMOS
G	- super high speed, more than 1 GHz

Many parts of the HC, AC, and FC families are available in ”T” versions, i.e. with input thresholds compatible with both TTL and 3.3 V CMOS signals.

CMOS LOGIC FAMILIES

74C Series
The 74C CMOS subfamily offers pin-to-pin replacement of the 74-series TTL logic functions. For instance, if 7400 is a quad two-input NAND in standard TTL, then 74C00 is a quad two-input NAND with the same pin connections in CMOS. The characteristic parameters of the 74C series CMOS are more or less the same as those of 4000-series devices.

CMOS LOGIC FAMILIES

74HC/HCT Series

The 74HC/HCT series is the high-speed CMOS version of the 74C series logic functions. This is achieved using silicon-gate CMOS technology rather than the metal-gate CMOS technology used in earlier 4000-series CMOS subfamilies. The 74HCT series is only a process variation of the 74HC series.

The 74HC/HCT series devices have an order of magnitude higher switching speed and also a much higher output drive capability than the 74C series devices. This series also offers pin-to-pin replacement of 74-series TTL logic functions. In addition, the 74HCT series devices have TTL-compatible inputs.

CMOS LOGIC FAMILIES

74AC/ACT Series

The 74AC series is presently the fastest CMOS logic family. This logic family has the best combination of high speed, low power consumption and high output drive capability. Again, 74ACT is only a process variation of 74AC. In addition, 74ACT series devices have TTL-compatible inputs.

REVISION QUESTIONS

1. Define the concept of logic family.

2. Explain the governing parameters of the logic families.

3. Describe the difference between the bipolar integrated circuits and MOS integrated circuits.

4. What is noise immunity? What is propagation delay?

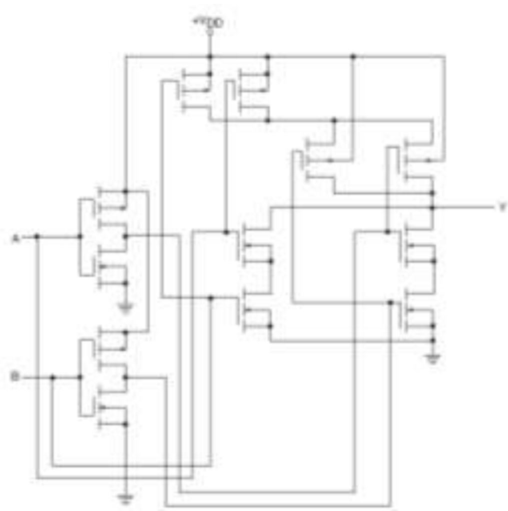
5. Describe the characteristics of MOS logic.

6. Describe enhancement type MOS and depletion type MOS with constructional details.

7. Draw a 3-input CMOS NAND gate. Repeat for a 3-input NOR gate with CMOS.

PROBLEMS AND EXERCISES

1. Write the logic expression for the CMOS circuit below.



PROBLEMS AND EXERCISES

2. Draw the transistor level CMOS complex gate circuit implementing

$$F = \overline{A\,B + C}$$

3. Draw the transistor level CMOS complex gate circuit implementing

$$F = \overline{(A + B)\,C}$$

NOTE ON SYMBOLS