DIGITAL TECHNICS II

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8. LECTURE: LOGIC CIRCUITS III: ECL, SCHOTTKY TTL, CMOS AND BiCMOS

2nd (Spring) term 2017/2018

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8. LECTURE

1. Digital IC technology picture gallery
2. Emitter coupled logic (ECL)
3. ”Classical” and high performance („advanced”) logic families, performance comparisons
4. Advanced Schottky TTL logic families
5. Advanced CMOS circuits and logic families
6. BiCMOS logic families

INTEGRATED CIRCUIT ETCHNOLOGY

Manufacturing technology of microelectronic (and MEMS) devices and chips.

Basic material: semiconductor single crystal (silicon,Si)

Processing:

Additive steps:

thin layer deposition – PVD, CVD, oxidation, patterning

Modification steps:

fotoexposition, ion implantation doping, thermal processing steps

Subtractive steps:

Chemical and physical etching steps, laser-assisted and mechanical layer removal

Wafer technology: Sequential application of the above steps and their combinations on the surface of the wafer

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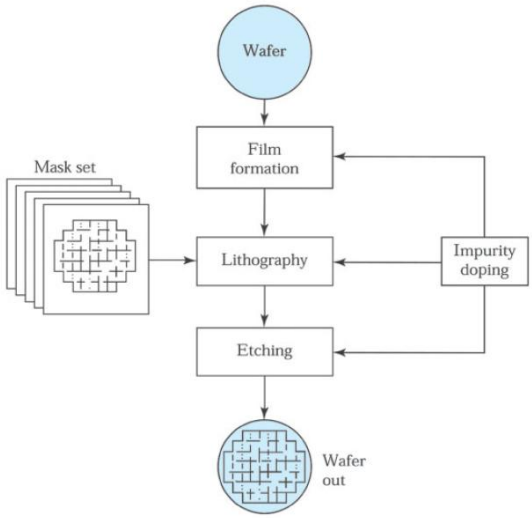
IC TECHNOLOGY FLOW DIAGRAM



Schematic flow diagram of IC fabrication

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SILICON INGOT AND WAFERS

300 mm (12 in.) dia ingot and polished silicon wafers

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TECHNOLOGY BASICS

Batch processing

10 to 50 thousands chips in one step.

Clean room in an IC fab

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HIGH CLEANNESS CONDITIONS

IC processing, especially lithography: only under very high cleanness conditions, clean room.

US Federal Standard: level100: less than 100 particle larger than 0.5 μm.

Submicron lithography: level10 and level 1 clean rooms. Extremely expensive!

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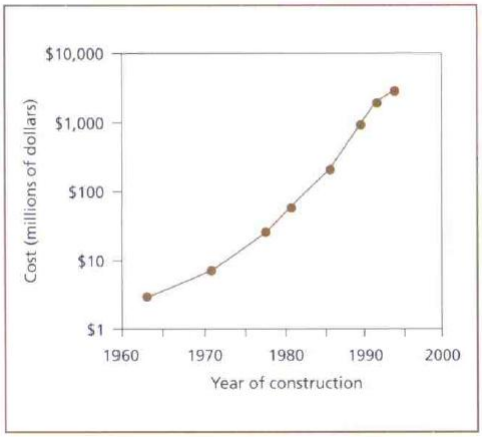
IC FAB COSTS



Cost of IC manufacturing clean rooms in function of time (calendar year)

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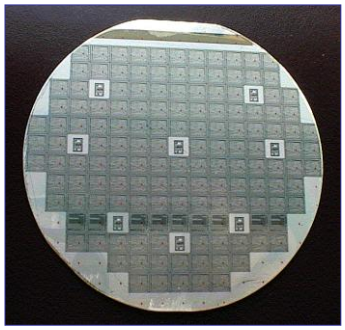
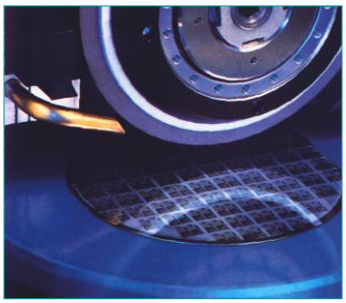
TECHNOLOGY BASICS

Wafer and chip: ca. 100-2000 chips are processed on a wafer simultaneously





Dicing of processed wafers

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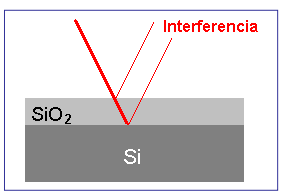
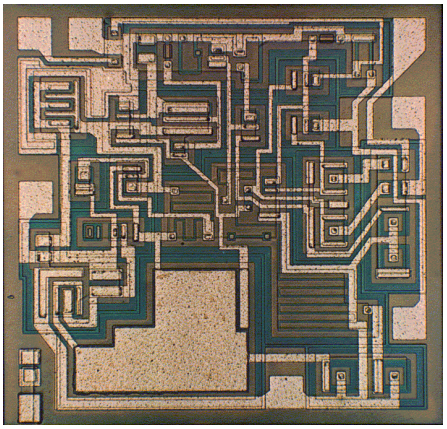
TECHNOLOGY BASICS

Optical microscope picture of a simple IC. Areas with diiferent oxide thickenss exhibit different colours (interference).





μA 741

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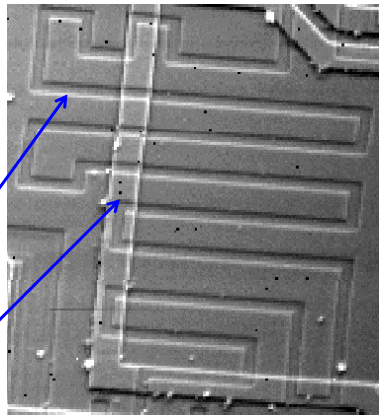
TECHNOLOGY BASICS

Strip width

Strip width at the beginning:
12 - 15 μm
Today (yesterday?) < 0,06-0,1 μm



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TECHNOLOGY BASICS

Masks:

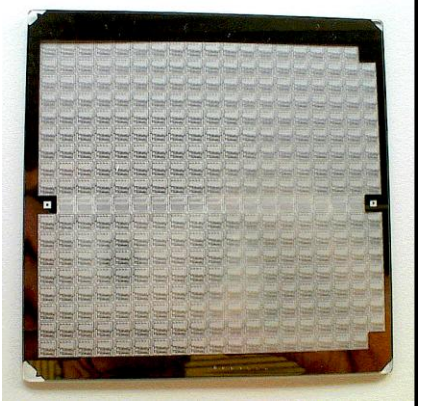
Cr layer on glass

Required accuracy e.g. 0,1 μm on 10 cm distance:

Relative accuracy 10^{-6}

Visible light: λ = 0,4-0,8 μm

Deep UV light is necessary for the processing (photolithography)



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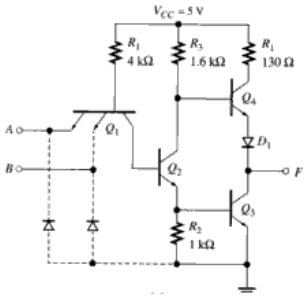
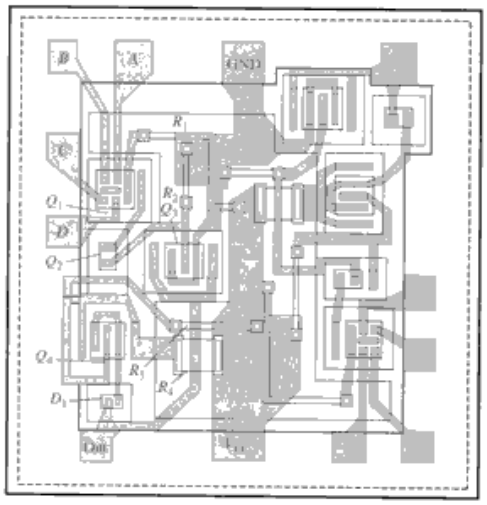
STANDARD TTL NAND GATE



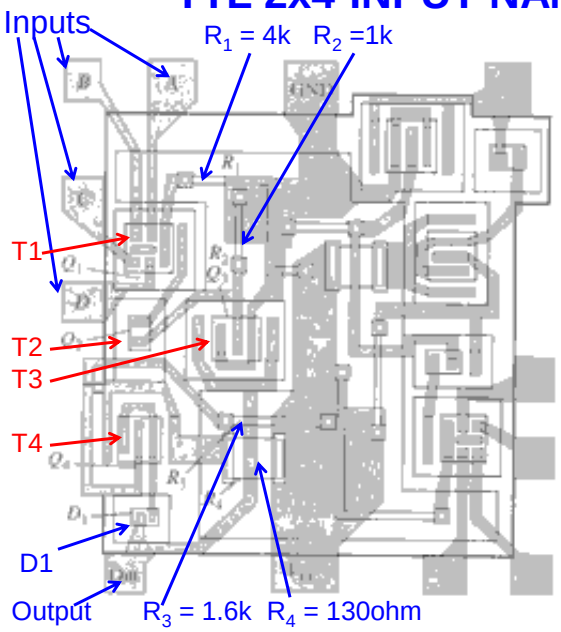


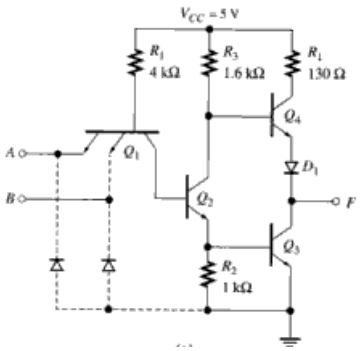
Standard 2-input TTL NAND gate circuit

Layout of dual 4-input NAND gate circuit

Size: emitter window of the input multiemitter transistor: 16x16 μmsq

TTL 2x4-INPUT NAND GATE





EMITTER COUPLED LOGIC (ECL)

The ECL family (also called current-mode logic, CML) is the fastest logic family in the group of bipolar logic families. The characteristic features that give this logic family its high speed or short propagation delay are outlined as follows:

1. It is a nonsaturating logic. That is, the transistors in this logic are always operated in the active region of their output characteristics. They are never driven to either cut-off or saturation, which means that logic LOW and HIGH states correspond to different states of conduction of various bipolar transistors. The main factor, limiting the switching speed of TTL type circuits, the minority carrier storage is not present or at least is very weak.

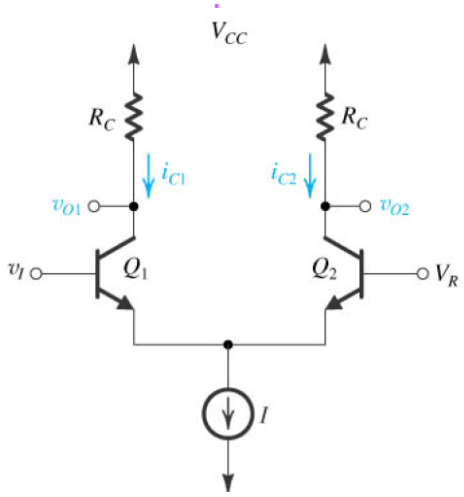
EMITTER COUPLED LOGIC (ECL)

2. The logic swing, that is, the difference in the voltage levels corresponding to logic LOW and HIGH states, is kept small (typically 0.85 V), with the result that the output capacitance needs to be charged and discharged by a relatively much smaller voltage differential.

3. The circuit currents are relatively high and the output impedance is low, with the result that the output capacitance can be charged and discharged quickly.

ECL DIFFERENTIAL PAIR

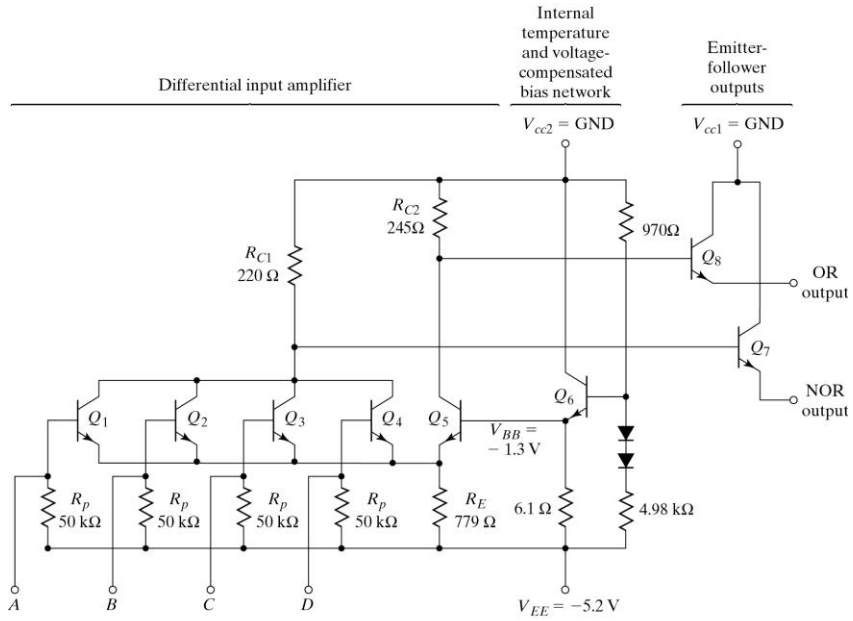
Emitter-coupled logic (ECL) is based on the use of the current-steering switch, most conveniently realised using this differential pair.



ECL FEATURES

Nonsaturated digital logic family
Propagation rate as low as 1-2ns
Used mostly in high speed circuits
Noise immunity and power dissipation is the worst of all logic families.
High level -0.8V, Low level -1.8V
Including
- Differential input amplifier
- Internal temperature and voltage compensated bias network
- Emitter-follower outputs

ECL BASIC GATE



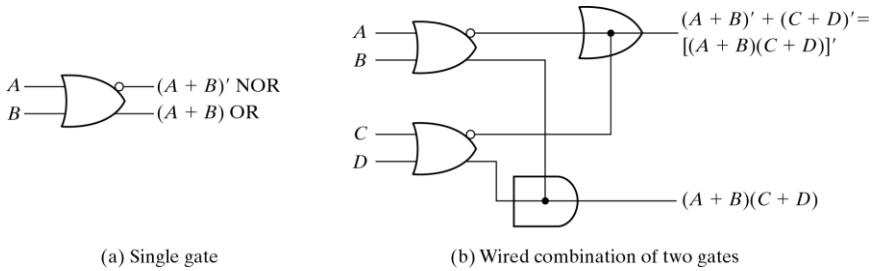
ECL BENEFITS

ECL gates produce both true and complemented outputs

ECL gates are fast since it the BJTs are always in forward active mode, and it only takes a few tenths of a volt to get the output to change states, hence reducing the dynamic power

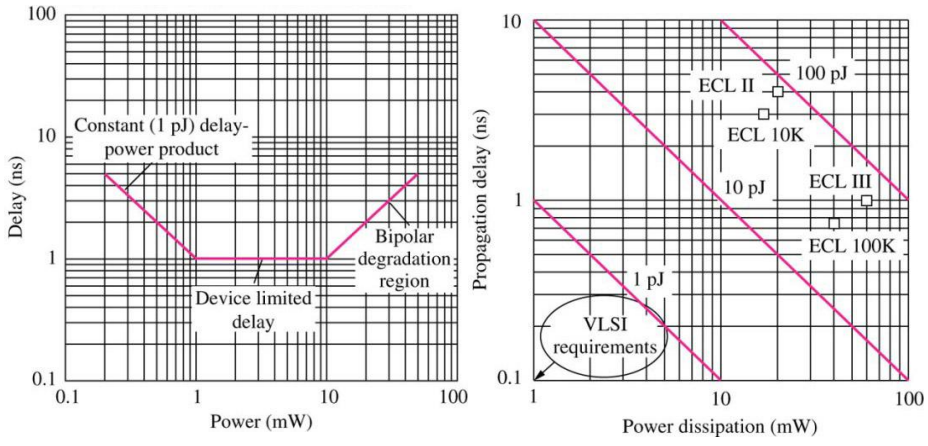
ECL gates provide near constant power supply current for all states thereby generating less noise from the other circuits

ECL GATE SYMBOLS



Graphic symbols of ECL gates

ECL: POWER-DELAY PRODUCT



Tradeoff of power and speed for ECL gates

ECL PERFORMANCE

Different subfamilies of ECL logic include among others MECL-I, MECL-II, MECL-III, MECL 10K, MECL 10H and MECL 10E.

As an example the basic characteristic parameters of MECL-10H are as follows:

- gate propagation delay=1 ns;
- flip-flop toggle frequency=250MHz (min.);
- power dissipation per gate=25 mW;
- delay–power product=25 pJ.

ECL PERFORMANCE

ECL performance is illustrated with data for 4 bit 10181 type adder without and with type 10179 fast carry unit

Number of bits	Add time (ns) no fast carry chip	Total add time (ns) with fast carry chip
4	8	
8	11	
16	17	16 (1 -79, 4 -81)
24	23	17 (1 -79, 6 -81)
32	30	19 (2 -79, 8 -81)
64	54	25 (4 -79, 16 -81)

COMPARISON OF LOGIC FAMILIES

Parameter	CMOS	TTL	ECL
Basic gate	NAND/NOR	NAND	OR/NOR
Fan-out	>50	10	25
Power per gate (mW)	1 @ 1 MHz	1 - 22	4 - 55
Noise immunity	Excellent	Very good	Good
t_{PD} (ns)	1 - 200	1.5 – 33	1 - 4

TRANSISTOR-TRANSISTOR LOGIC TTL

The original basic TTL gate was a slight improvement over the DTL gate.

There are several TTL subfamilies or series of the TTL technology.

Has a number start with 74 and follows with a suffix that identifies the series type, e.g. 7404, 74S86, 74ALS161.

Three different types of output configurations:

1. open-collector output
2. Totem-pole output
3. Three-state (or tristate) output

74 – standard

54 – military

84 – industrial (discontinued)

TTL SERIES

• STANDARD		OBSOLOTE!
• SCHOTTKY	S	IN DECLINE/OBSOLOTE
• LOW-POWER SCHOTTKY	LS	IN DECLINE/OBSOLOTE
• ADVACED SCHOTTKY	AS	IN DECLINE
• FAST ADVANCED SCHOTTKY	F	
• ADVACED LOW-POWER SCHOTTKY	ALS	

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HIGH SPEED/HIGH PERFORMANCE LOGIC COMPONENTS

Components for today's high-speed systems:

- Advanced Schottky transistor-transistor logic (TTL)
- Advanced complementary metal-oxide semiconductor (CMOS)
- Bipolar combined with CMOS (BiCMOS)

SCHOTTKY TTL: AN INTRODUCTION

Transistor in bipolar logic (standard TTL) are saturated switches - minority carrier storage limits the speed of the device.

Variations of the standard TTL design to reduce these effects and improve speed, power consumption, or both.

”Schottky transistors” i.e. junction transistors with integrated Schottky barrier clamping diodes between the collector and basis reduce or prevent charge storage, leading to faster switching gates.

Incorporating Schottky barrier diodes into the TTL design, the switching speed can be reduced to 2 ... 5 nsec, a half or full order of magnitude improvement with respect to conventional design.

SCHOTTKY DIODE I-V CHARACTERISTICS

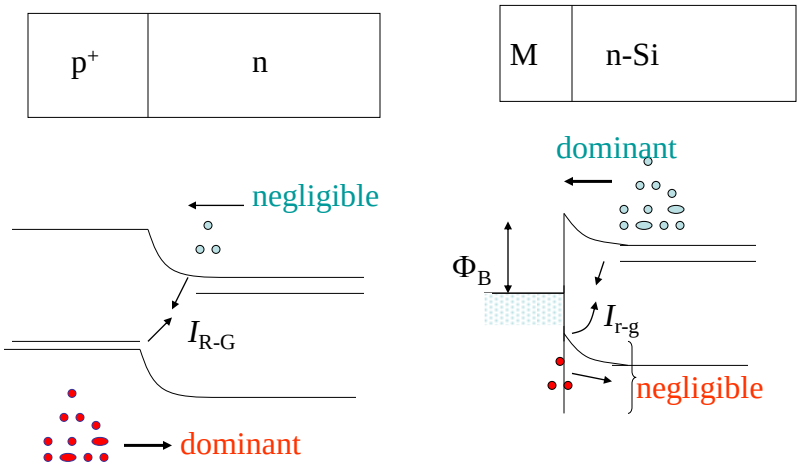
- Schottky diode is a metal-semiconductor (MS) diode
- Historically, Schottky diodes are the oldest diodes
- MS diode electrostatics and the general shape of the MS diode I-V characteristics are similar to p^+n diodes, but the details of current flow are different.
- Dominant currents in a p^+n diode

– arise from recombination in the depletion layer under small forward bias.
– arise from hole injection from p^+ side under larger forward bias.

- Dominant currents in a MS Schottky diodes

– Electron injection from the semiconductor to the metal.

CURRENT COMPONENTS IN p^+n and MS SCHOTTKY DIODES



I-V CHARACTERISTICS

$$I = I_S\left(e^{\frac{qV_A}{kT}} - 1\right) \quad \text{where} \quad I_S = A\mathcal{A}^* T^2 e^{-\frac{\Phi_B}{kT}}$$

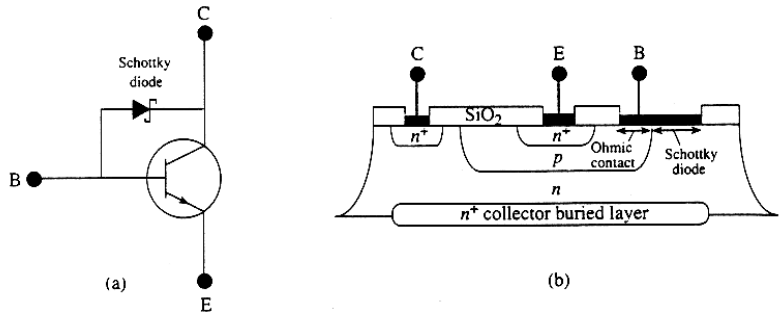
where Φ_B is Schottky barrier height, V_A is applied voltage, A is area, and A^* is Richardson's constant.

The reverse leakage current for a Schottky diode is generally much larger than that for a p^+n diode.

Since MS Schottky diode is a majority carrier devices, the frequency response of the device is much higher than that of equivalent p^+ n diode.

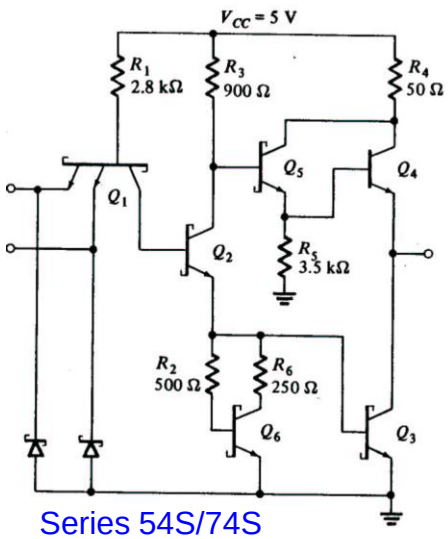
SPEEDING UP THE SWITCHING TRANSIENTS: SCHOTTKY TTL

The collector is ”clamped” by a Schottky diode. This prevents the transistor reaching deep saturation.



High speed variant of TTL
Schottky transistors which have faster switching speed
Schottky-barrier diode connected from base to collector to prevent transistor from going into saturation

BASIC SCHOTTKY TTL NAND GATE

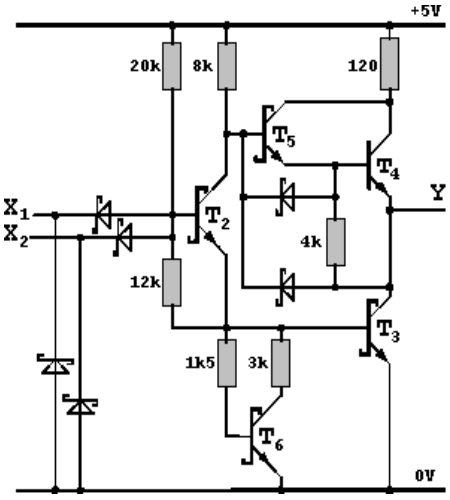


Series 54S/74S
t_{pd} = 3 nsec, P = 19 mW

Features:

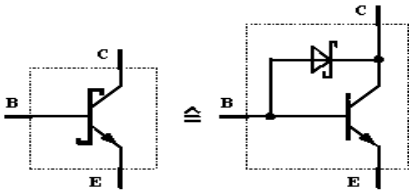
Transistors: all clamped with Schottky diode except Q4 (this does not saturate)
Input diodes: high-speed clamping of input signal excursions below ground
Q5: Emitter follower to speed up 0-to-1 switching of output
50 ohm resistor: Low-to-high transient switching current reduction and impedance matching

LOW-POWER SCHOTTKY



Basic NAND gate with LS-(*Low-Power-Schottky*) Technology

Note: input diodes NOT multi-emitter transistor



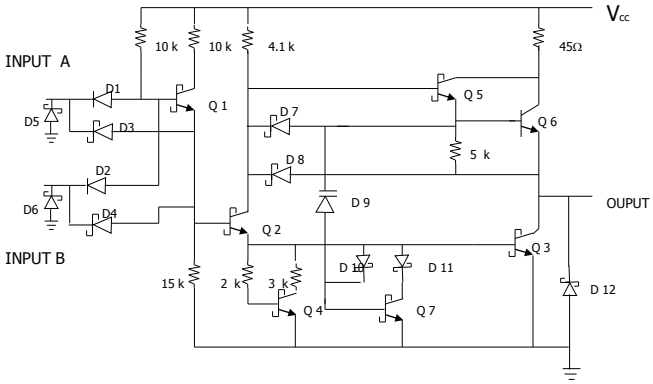
Series 54LS/74LS
t_{pd} = 9.5 nsec, P = 2 mW

ADVANCED SCHOTTKY TTL LOGIC FAMILIES

- Letter designator
  - F: fast advanced Schottky TTL
  - ALS: advanced low-power Schottky TTL
  - AS: advanced Schottky TTL
- Selection criteria of FAST vs. AS
  - Price, availability

ADVANCED SCHOTTKY TTL CIRCUITS (1)

- 74F00 NAND

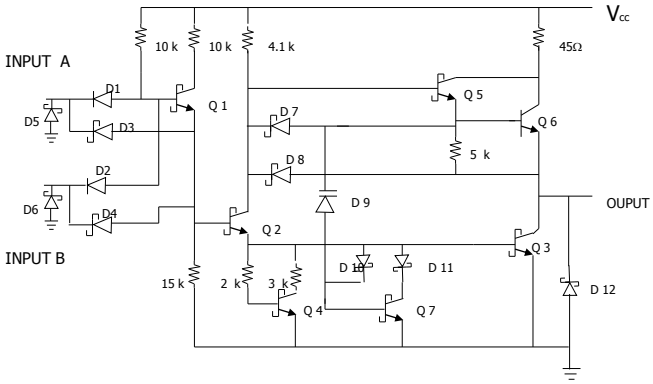


Input circuit
Component function
D1, D2: AND function
D5, D6: High-speed clamping of input signal excursions below ground
D3, D4: Stored charge removal of the base of Q2 on negative transition of the input
10KΩ resistor connected to D1 and D2: Small amount of current source

Series 54F/74F
t_{pd} = 3 nsec, P = 6 mW

ADVANCED SCHOTTKY TTL CIRCUITS (2)

- 74F00 NAND



Output circuit
Q5, Q6: Darlington pair
45Ω resistor: Low-to-high transient switching currents reduction and impedance matching
D12: negative voltage excursions reductions due to reflection caused by transmission-line effects

Series 54F/74F
t_{pd} = 3 nsec, P = 6 mW

CMOS AND ADVANCED CMOS: SURVEY

C - 4-15 V operation (similar to 4000 series)
HC - High speed, similar performance to LS
HCT - high speed, compatible logic levels to bipolar parts
AC - Advanced, performance generally between S and F
AHC - Advanced high speed, 3x faster than HC
FC - Fast, performance similar to F
LCX - 3V supply and 5 volt tolerant inputs
LVQ - Low voltage 3.3 V
LVX - Low voltage 3.3 V with 5 V tolerant inputs
VHC - very high speed „S" performance in CMOS
G - super high speed, more than 1 GHz

Many parts of the HC, AC, and FC families are available in "T" versions, i.e. with input thresholds compatible with both TTL and 3.3 V CMOS signals.

BiCMOS LOGIC

One major improvement was to combine CMOS inputs and logic and TTL drivers to form a new type of logic circuits called BiCMOS family.
In the early to late 1990s
BiCMOS technology
CMOS input structure + CMOS internal logic + Bipolar (npn transistor) output structure
high speed, high drive, low power
applications: internal bus, output interface, etc.
Common types:

BCT – BiCMOS, TTL compatible input thresholds
ABT – Advanced BiCMOS, TTL compatible input thresholds, faster than BCT

BiCMOS

BiCMOS represents an up-to-date technology.
It combines the advantages of current-controlled (BJT) and voltage-controlled devices.
It makes possible to use on one chip the optimal device and technology for each task.

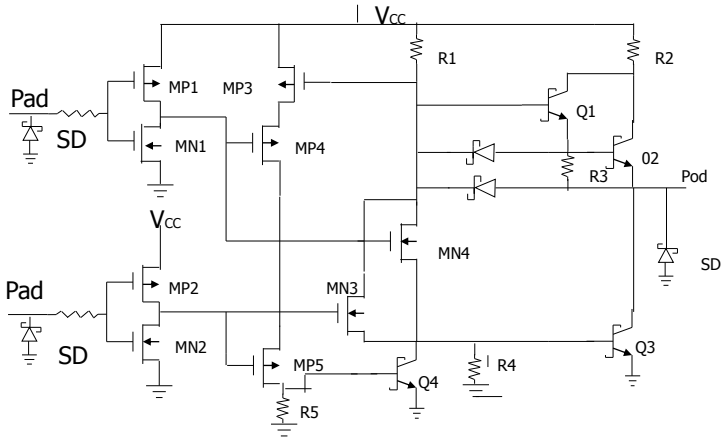
Application ⇒ VLSI & ULSI digital and mix-mode circuits.
BiCMOS is approximately 2 to 2.5 times faster than CMOS, if it is used properly. If it is not used properly, BiCMOS could be slower than CMOS and consumes more power.

E.g. the 60 MHz Intel Pentium (586) microprocessor was fabricated with 0.8 μm gate length MOS transistors in BiCMOS technology. The 2x2 cm^2 chip (270 input/output) contains more than 3 million transistors.

BiCMOS LOGIC CIRCUITS (1)

Transistor count: NMOS 4, PMOS 5, BJT 4

74BC00 NAND



BiCMOS LOGIC CIRCUITS (2)

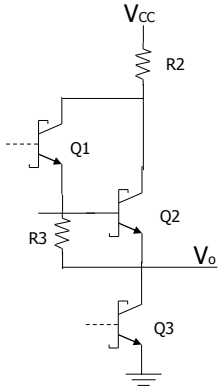
- Bipolar totem-pole output stage
  - Advantage
    - By totem-pole stage output voltage swing
      - Less dynamic power
      - Less crosstalk
      - Less transient switching current
        - » Less ground bounce, less power and reference level corruption

BiCMOS LOGIC CIRCUITS (3)

- By resistor R2
  - Reduction of low-to-high transient switching current
  - Low-to-high output impedance matching to PCB trace
- More stable with temperature than MOSFETs
  - In CMOS, when 1°C increases
    - » 6% impedance change
    - » 3% speed change (slow down)

BiCMOS LOGIC CIRCUITS (4)

- Theoretical totem-pole voltage swing limit
  - 3.4V due to Darlington pull-up output transistor
- Why is a measurement voltage higher than 3.4V?
  - Stabilization after overshoot
  - Leakage currents



BiCMOS: APPLICATION EXAMPLES

Carry look ahead in adders: the carry can be calculated from the *generate* and *propagate* combinations. Fast operation is ensured by using bipolar output stages in the implementation of

$$C_{i+1} = G_i + P_i C_i$$

allowing a fast charging of the loading capacitances.

Other example is the driving of buses, which also represent relatively large capacitive loads.

FIGURE-OF-MERIT: POWER-DELAY PRODUCT

The product of the average power consumption and average propagation delay. Since the clock cycle is limited by the propagation delay, this number is essentially the typical energy consumption per cycle per gate.

Values are currently in the picoJoule range.

On thing that makes this a good *figure-of-merit* is that many of the simple things one can do to improve (decrease) propagation delay essentially increases (degrades) the current and thus the power consumption, so the PDP remains constant.

POWER-DELAY PRODUCT

”Good” circuit: small delay and small power dissipation.

Figure-of-merit: the product of these two parameters (power-delay product).

Standard 54/74 series: t_{pd} = 10 nsec, P = 10 mW/gate

$$P\, t_{pd} = 100 \text{ pJ}$$

Interpretation: approximately the energy needed to change the value of 1 bit.

SCHOTTKY TTL: POWER-DELAY PRODUCT

54S/74S series: t_{pd} = 3 nsec, P = 19 mW/gate

$P\ t_{pd}$ = 57 pJ

54LS/74LS series: t_{pd} = 9 nsec, P = 2 mW/gate

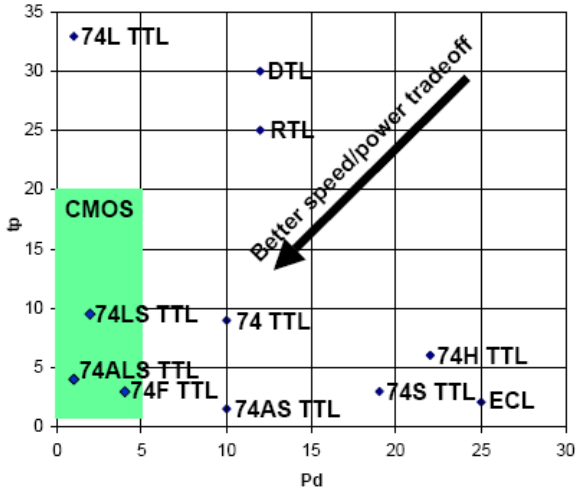
$P\ t_{pd}$ = 18 pJ

A factor of 1.5 and 5 better than standard TTL!

TTL AND CMOS: Pτ FIGURE OF MERIT

Circuit family	Propagation delay t_{pd} [ns]	Gate dissipation P_d [mW]	„Jósági" tényező P_d*t_{pd} [pJ]
74xx	10	10	100
74LSxx	9.5	2	19
74ASxx	1.5	2	13
74ALSxx	4	1.2	5
74Fxx	3	6	18
74HCxx	8	0.003	24×10^{-3}
74HCTxx	14	0.003	42×10^{-3}
74ACxx	5	0.010	50×10^{-3}
74ACTxx	5	0.010	50×10^{-3}
74AHCxx	5.5	0.003	16×10^{-3}
74AHCTxx	5	0.003	14×10^{-3}
10xxx	2	25	50
10Hxxx	1	25	25

LOGIC FAMILY TRADEOFF



Propagation delay versus power dissipation

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FET (MOSFET) PHYSICAL SPEED LIMIT

Absolute upper limit for all transit-time type devices: transit time or transit frequency

$$f_{max} \leq f_t = 1 / (2 \pi \tau_t) \quad \text{(unity gain!)}$$

Si 0.8 µm MOS transistor (Intel Pentium, 60 MHz):

$v_{sat} = 5x10^6$ cm/sec (electrons) (Si material parameter)
$L_{gate} = 0{,}8$ µm
$\tau_t = L_{gate} / v_{sat} = 16$ psec

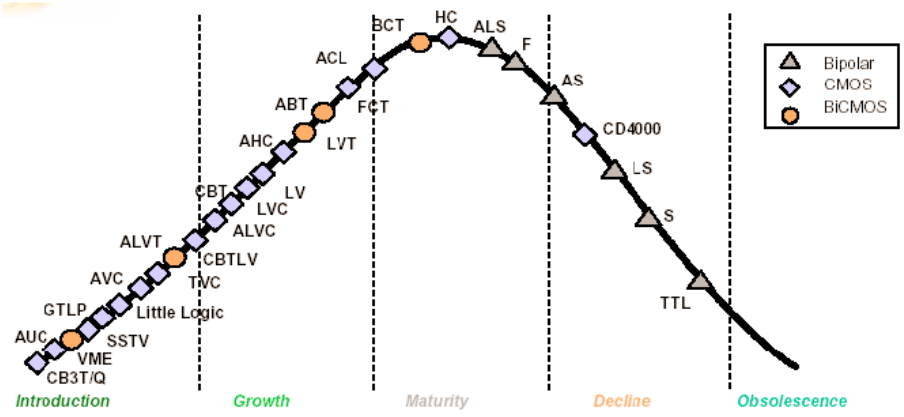
$$f_{max} \leq 10 \text{ GHz (unity gain)}$$

Clock frequency is much less of course! E.g. $f_{3dB} > f_{clock}$
To avoid distorsion minimum 3rd harmonic is necessary!

BIPOLAR AND MOS COMPARISON

Property	Bipolar	MOS
Power dissipation	medium	very small
Switching time	very small	relatively small
Input impedance	small	extremely large
Loading capability	good	very good
Noise	small	very small
Fab technology	more complex	more simple
Integration	less (in principle)	very high

LIFE CYCLE OF LOGIC CIRCUIT FAMILIES



REVISION QUESTIONS

1. Why is ECL called nonsaturating logic? What is the main advantage accruing from this? With the help of a relevant circuit schematic, briefly describe the operation of ECL OR/NOR logic.

2. What are the Schottky diode and Schottky transistor?

3. What is Bi-CMOS logic? What are its advantages?

4. Draw the basic BiCMOS inverter and explain.

5. Compare the characteristics of different logic families.

REVISION QUESTIONS

6. Explain the concept of power-delay product as a figure of merit.

7. Compare the standard TTL, low-power Schottky TTL and Schottky TTL on the basis of speed and power dissipation.