DIGITAL TECHNICS II

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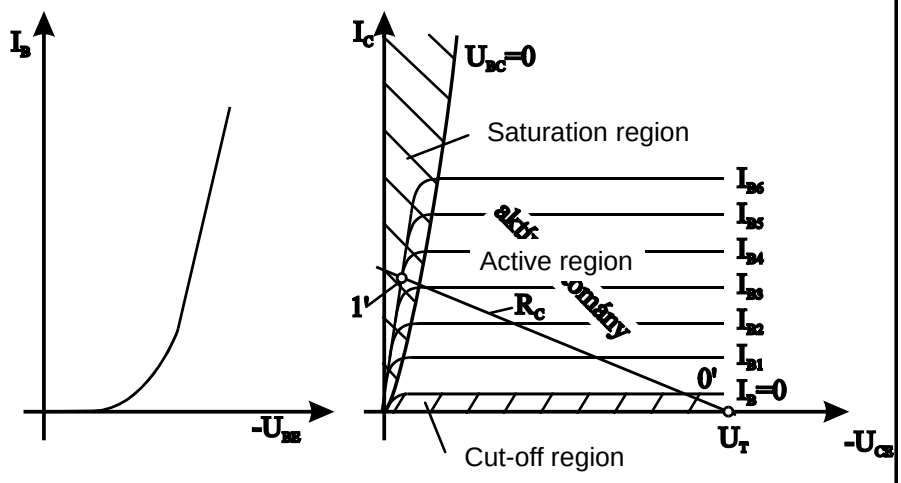
8a. LECTURE: DIGITAL CIRCUITS IIa: BASIC CIRCUITS (BIPOLAR)

2nd (Spring) term 2017/2018

1

SWITCHING MODE OPERATION OF BIPOLAR JUNCTION TRANSISTOR



2

SWITCHING MODE OPERATION OF BIPOLAR JUNCTION TRANSISTOR

Closed state ($U_{BE} < U_{op}$, $I_B \approx 0$), $I_C = I_{CEo}$, this current is neglible (small) in low-power Si transistors.

Fully opened state ($U_{BE} > U_{op}$), $U_{CE} = U_{CEsat}$ (≈ 0.1-0.2 V), the transistor is in saturated state.

Saturation $I_B > I_C/B$ or with safety margin $I_B >> I_C/B$

B – large signal current amplification factor

Region	V_{BE} (V)	V_{CE} (V)	Current Relation
Cutoff	< 0.6	Open circuit	$I_B=I_C=0$
Active	0.6-0.7	> 0.8	$I_C = h_{FE} I_B$
Saturation	0.7-0.8	0.2	$I_B \geq I_C/h_{FE}$

3

BIPOLAR TRANSISTOR IN SATUARTION

In saturation the collector-base diode is biased (slightly…) in forward direction (inverse mode)!

Si NPN transistor in saturation:

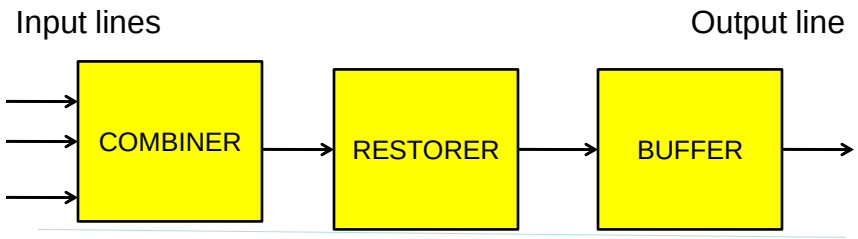
emitter	0 V
base	+ (0.6-0.65) V
collector	+ (0.10-0.15) V

The BC diode is forward biased with app. 0.5 V!

Consequences: diffusion capacitance, charge storage, storage time (switching delay), etc.

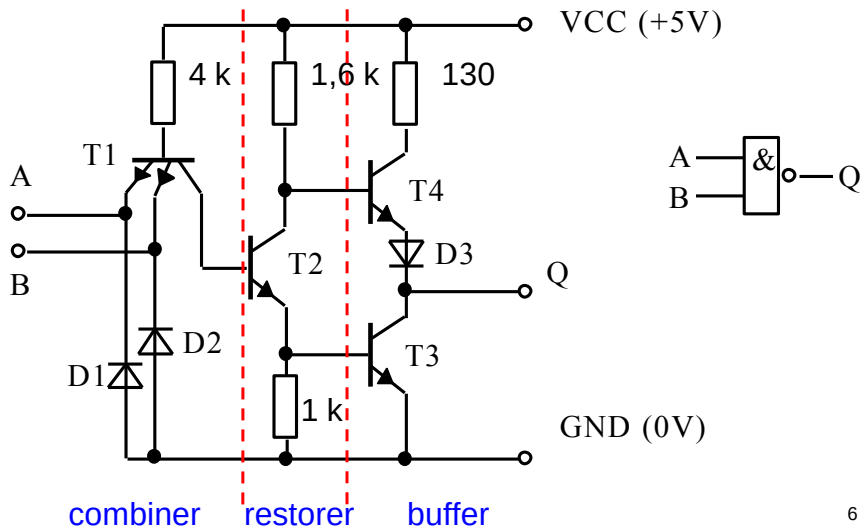
4

GATE CIRCUITS: GENERAL ARCHITECTURE



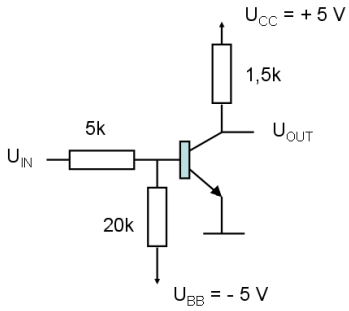
Generic circuit layout of digital gates

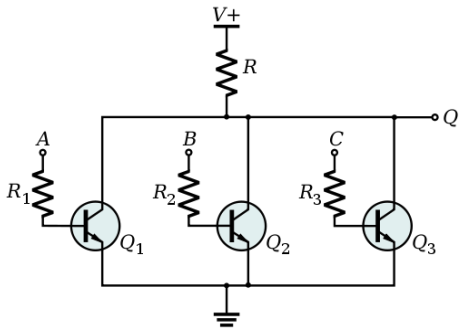
DEMO: STANDARD TTL GATE ARCHITECTURE



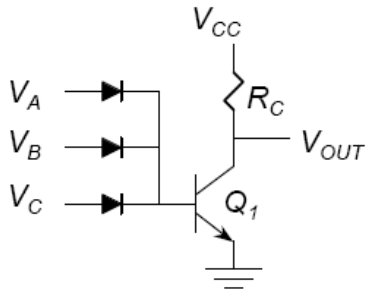
6

RESISTOR-TRANSISTOR LOGIC



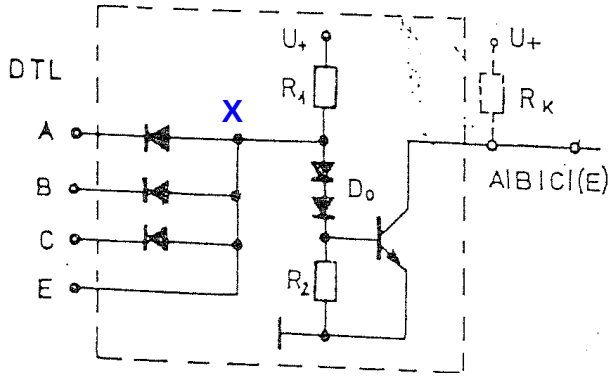


DTL: DIODE-TRANSISTOR LOGIC



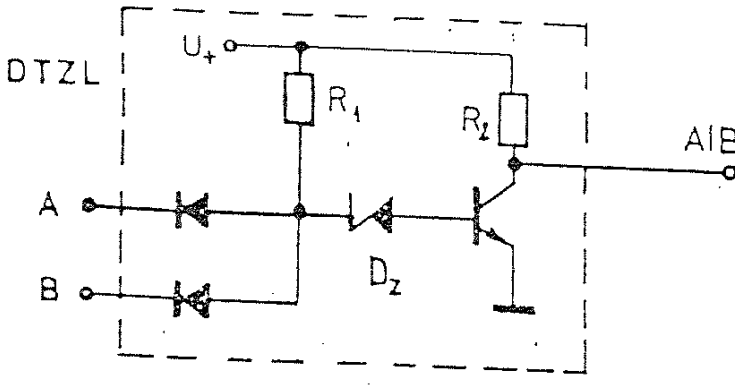
Generic (basic) layout.
If any input goes HIGH, the transistor conducts and saturates, V_{OUT} goes LOW.
If all inputs are LOW, the transistor cut off, and V_{OUT} goes HIGH.

BASIC DTL NAND GATE



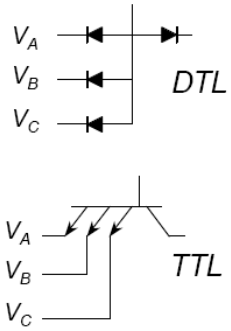
If all inputs are HIGH, Vx = ~2.2 V, and the transistor is open and saturated. If any input goes low (0-0.2 V), Vx = 0.7-0.9 V, and the transistor is cut-off.
The R2 resistor provides a discharge path for stored base charge in the BJT to provide a reasonable t_{PLH}.

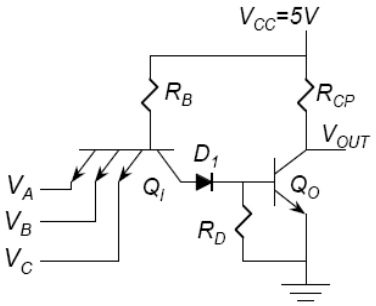
DTZL: DIODE TRANSISTOT (ZENER) LOGIC



Diode transistor (Zener) logic (DTZL), NAND gate

TTL: TRANSISTOR-TRANSISTOR LOGIC



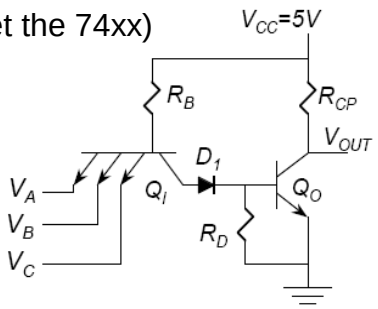


Why TTL?
The DTL input uses a number of diodes which take up considerable chip area.
In TTL, a single multi-emitter BJT replaces the input diodes, resulting in a more area-efficient design.

11

TTL: TRANSISTOR-TRANSISTOR LOGIC

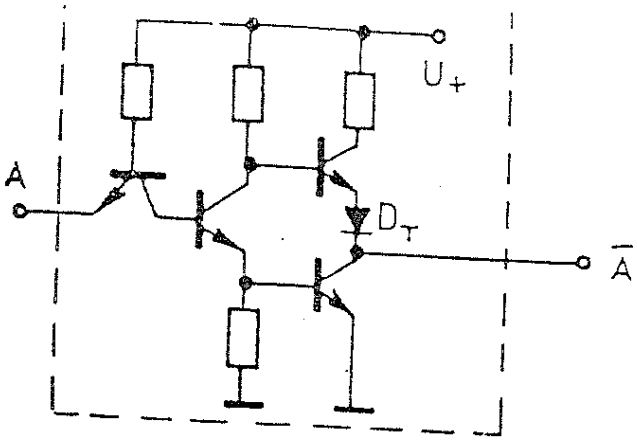
Basic TTL NAND gate (not yet the 74xx)



ALL INPUTS HIGH,
- Q1 is reverse actice
- Q2 is saurated
- $V_{OL} = V_{CES}$

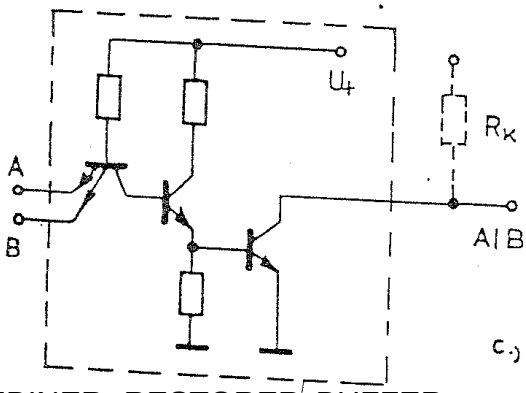
ANY INPUT LOW
- Q1 is saturated
- Q2 is cut-off
- $V_{OH} = V_{CC}$

TTL: THE (BASIC) INVERTER



COMBINER RESTORER BUFFER

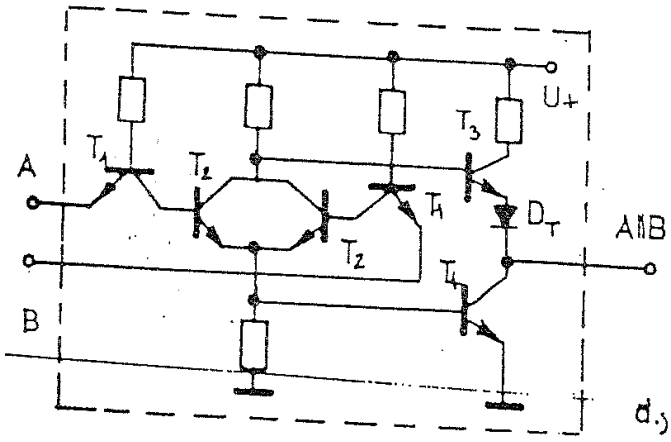
TTL: THE (OPEN COLLECTOR) NAND GATE



COMBINER RESTORER BUFFER

Transistor transistor logic (TTL), NAND gate (open-collector output)

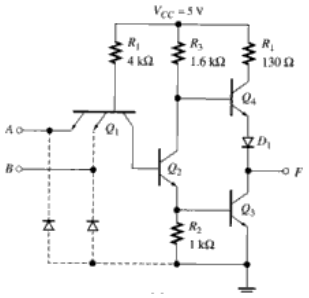
TTL: THE NOR GATE

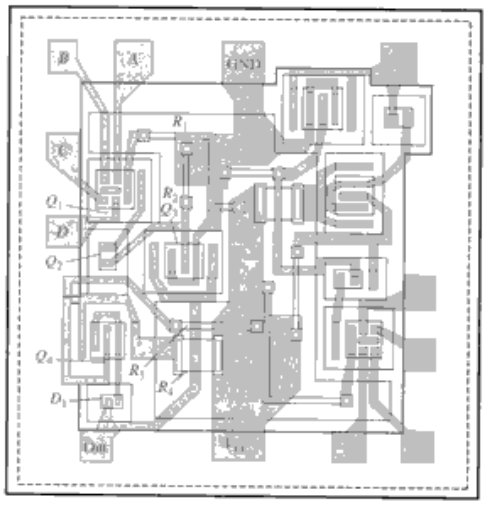


Transistor transistor logic (TTL), NOR gate (totem-pole output)

END OF LECTURE

STANDARD TTL NAND GATE

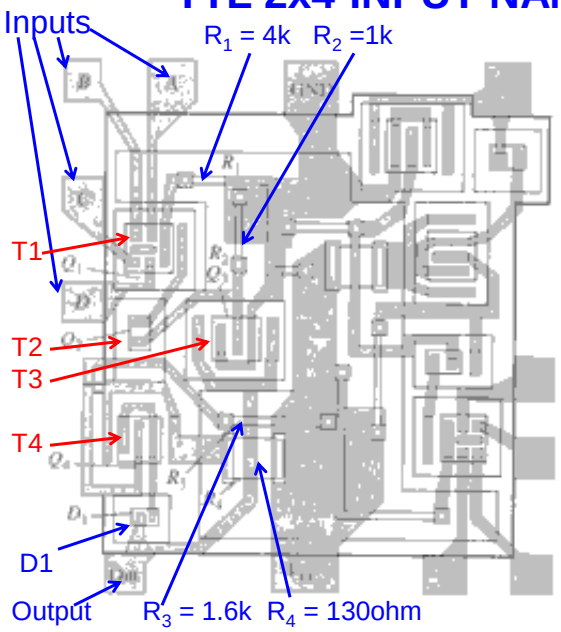


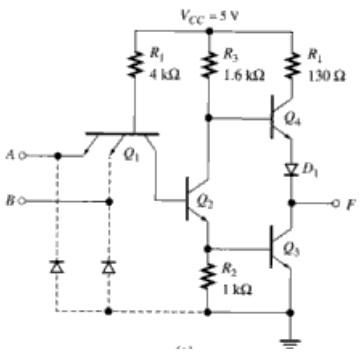


Standard 2-input TTL NAND gate circuit

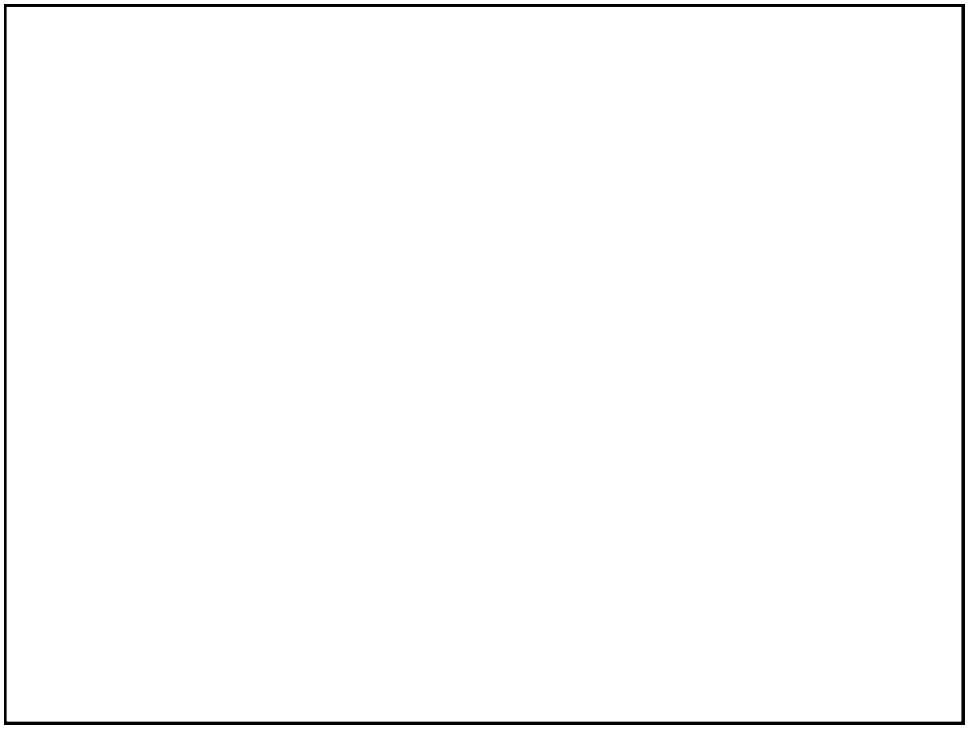
Layout of dual 4-input NAND gate circuit
Size: emitter window of the input multiemitter transistor: 16x16 μmsq

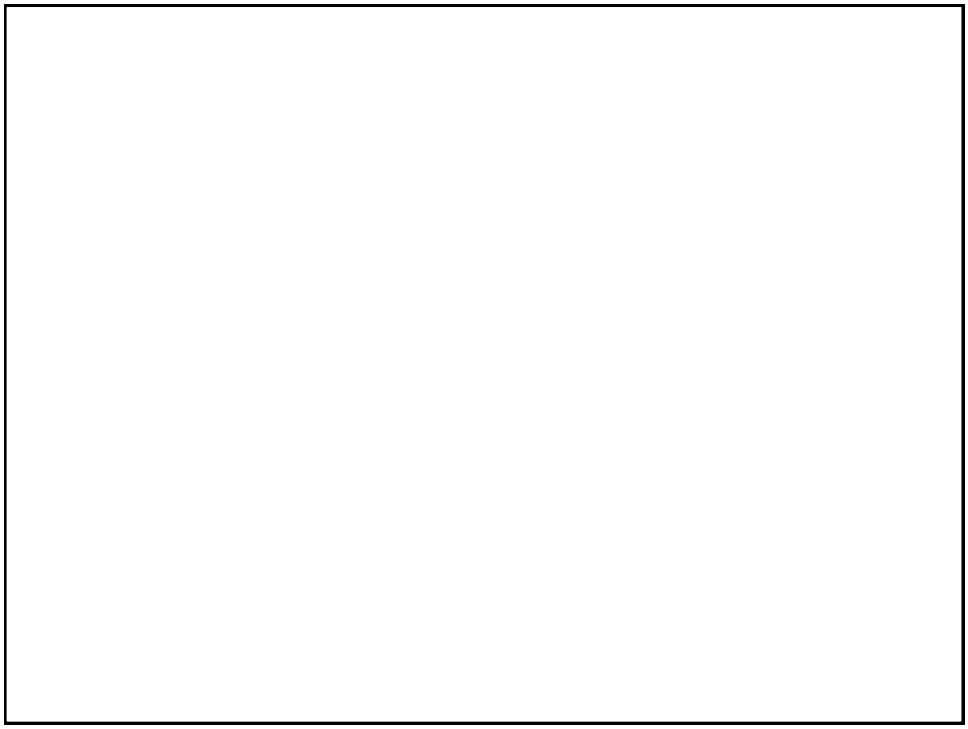
TTL 2x4-INPUT NAND GATE

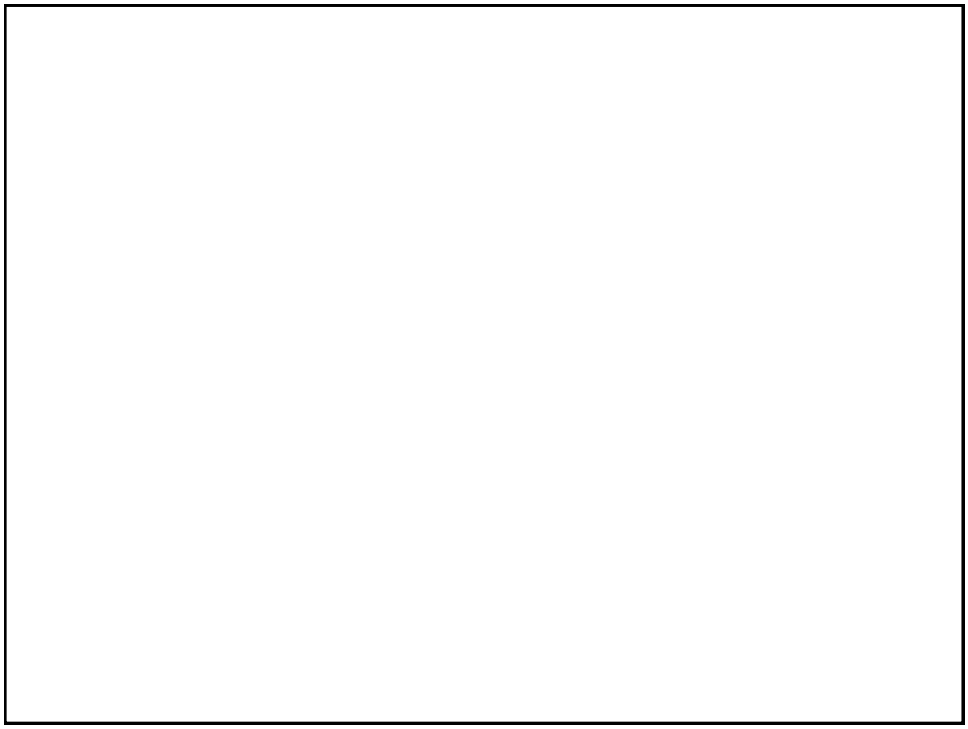


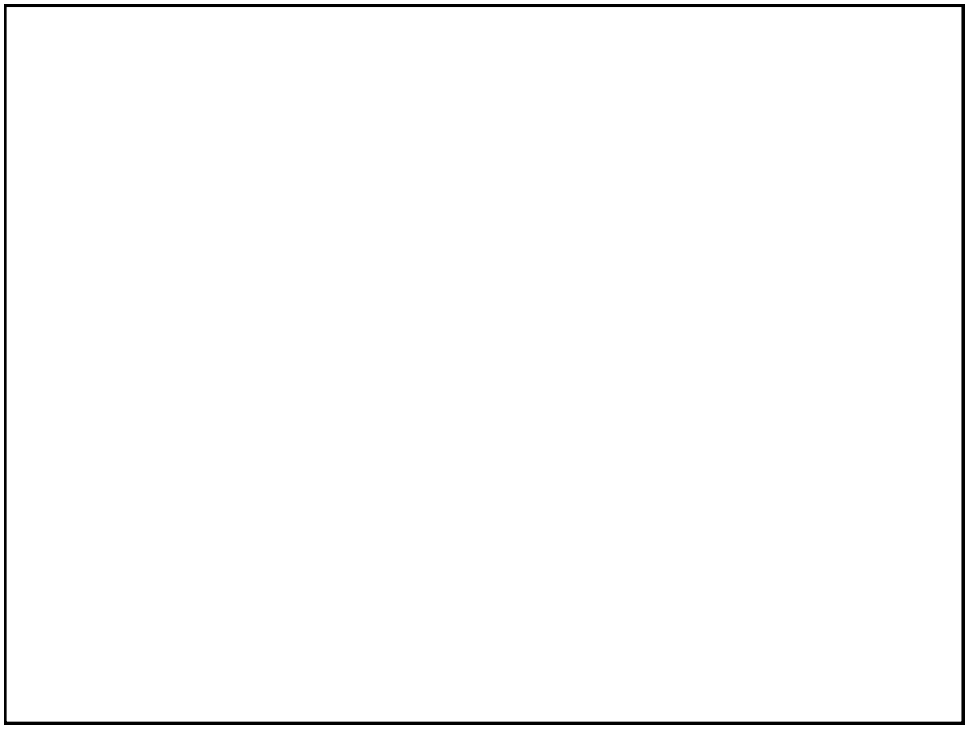


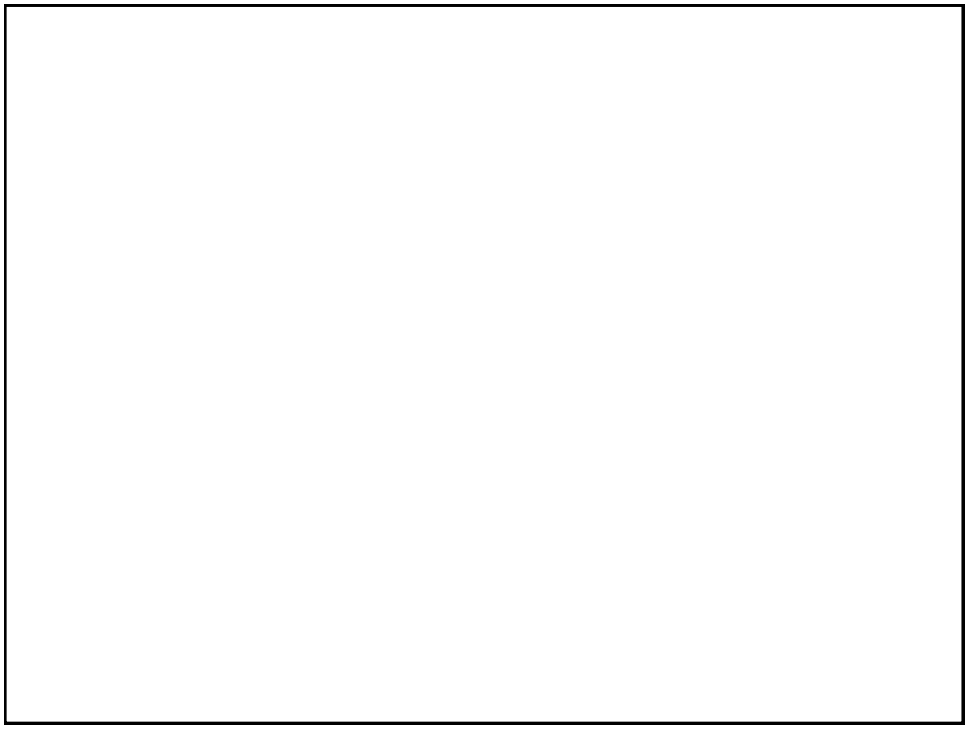
8a. LECTURE

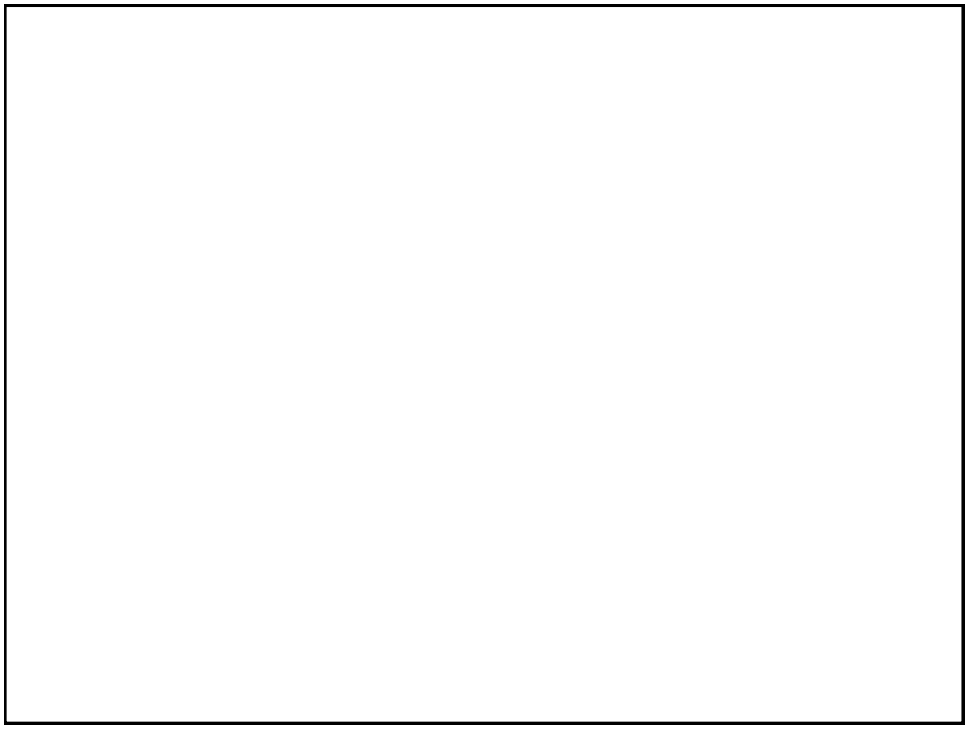


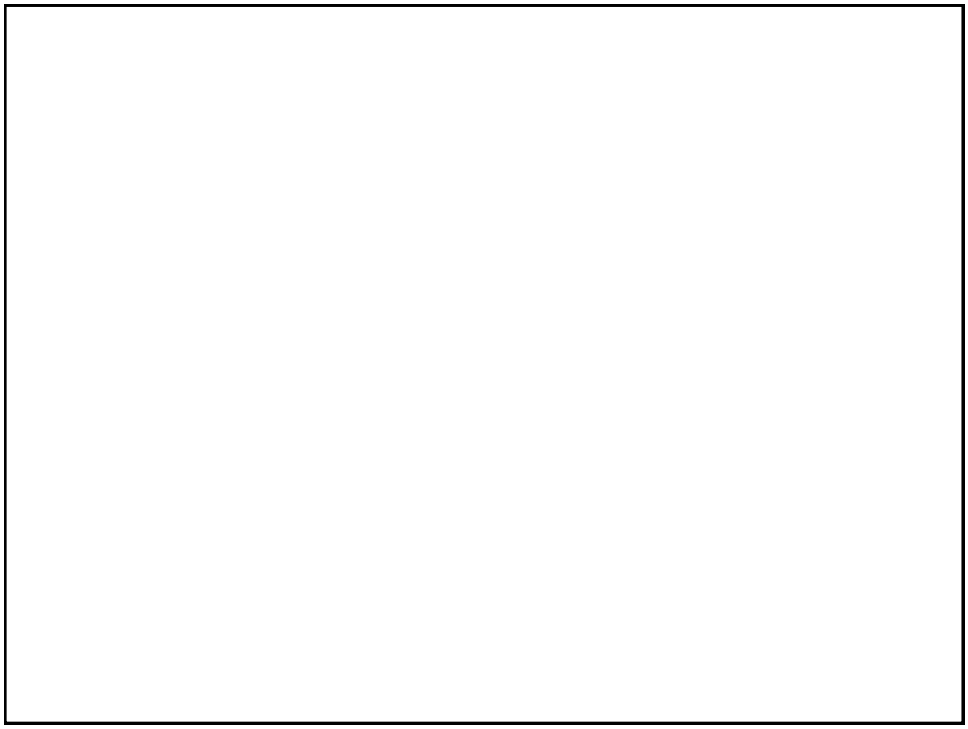


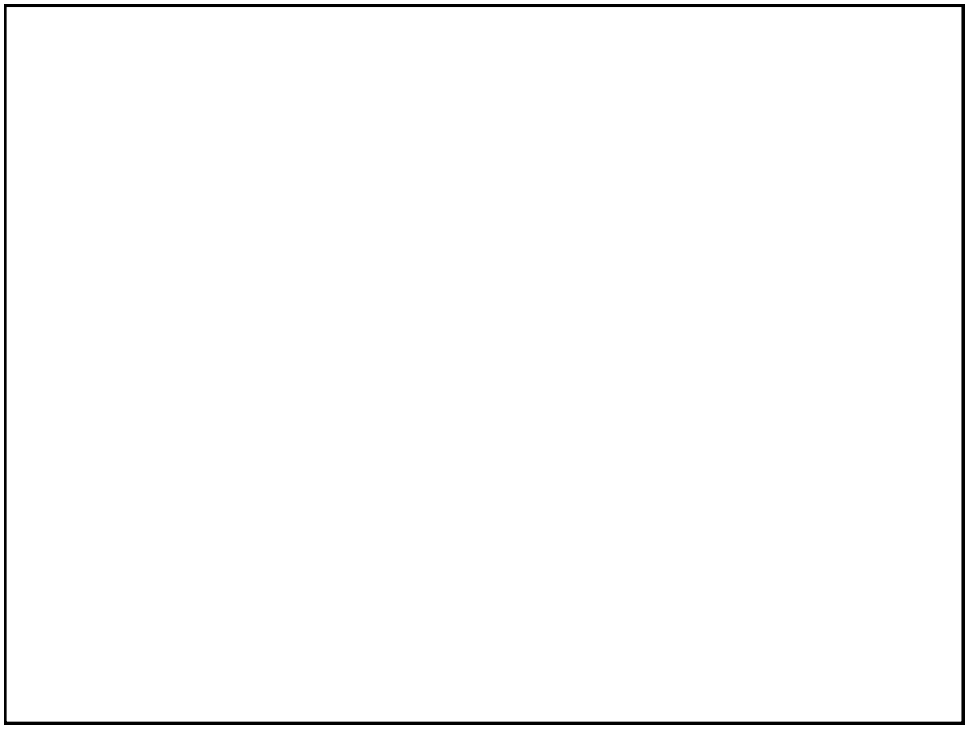


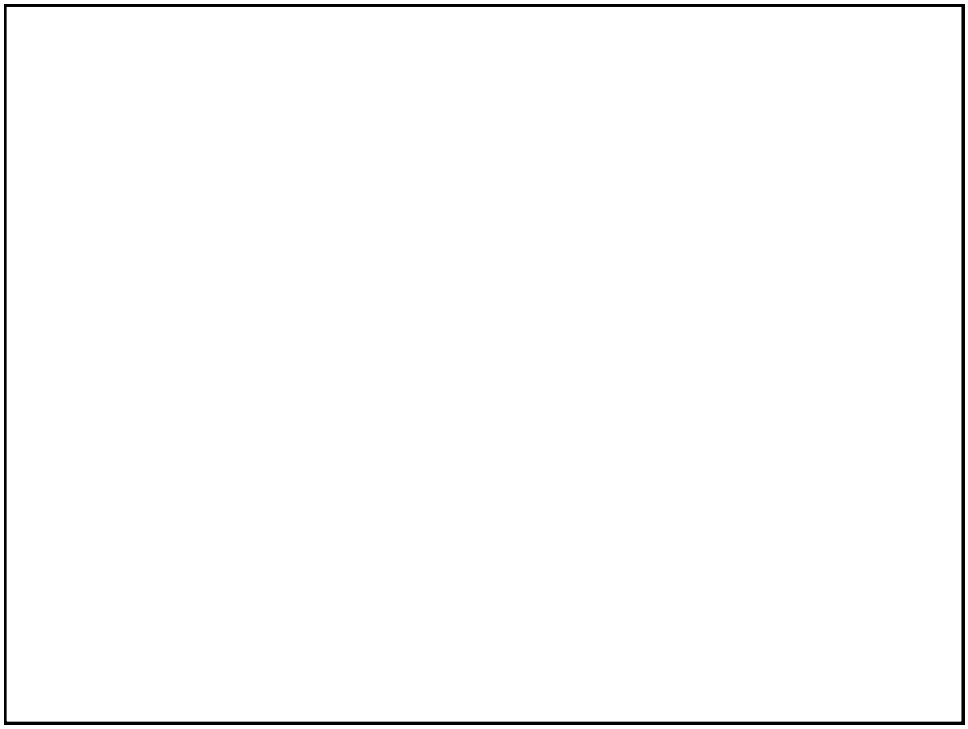


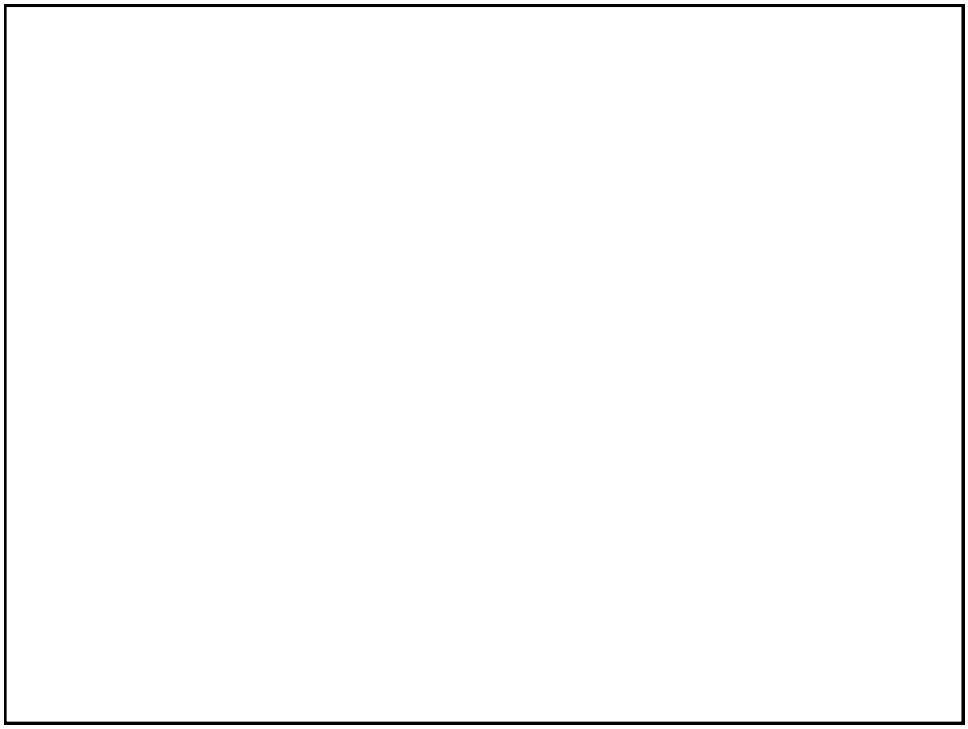












END OF LECTURE