NANO

MIKRO- ES NANOTECHNIKA II

Dr. Pődör Bálint

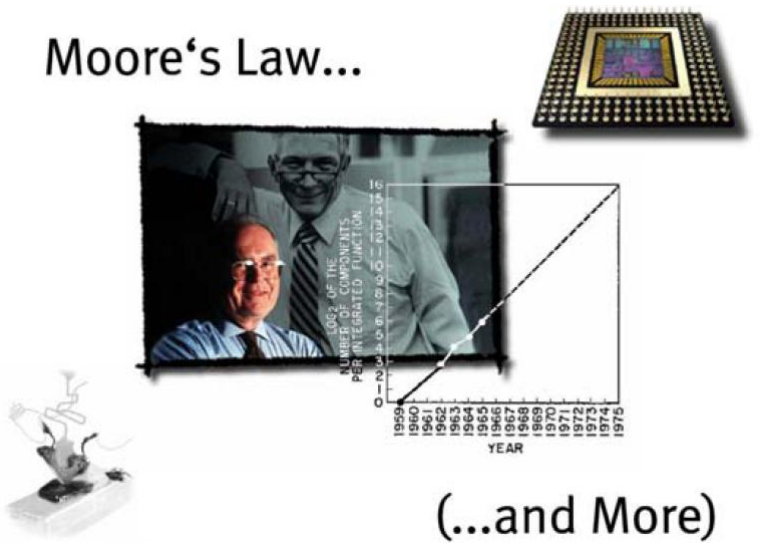
Óbudai Egyetem KVK Mikroelektronikai és Technológia Intézet

8. ELŐADÁS: NANOELEKTRONIKA II: ESZKÖZÖK NANOSKÁLÁN, Si, CNT, GRAFÉN

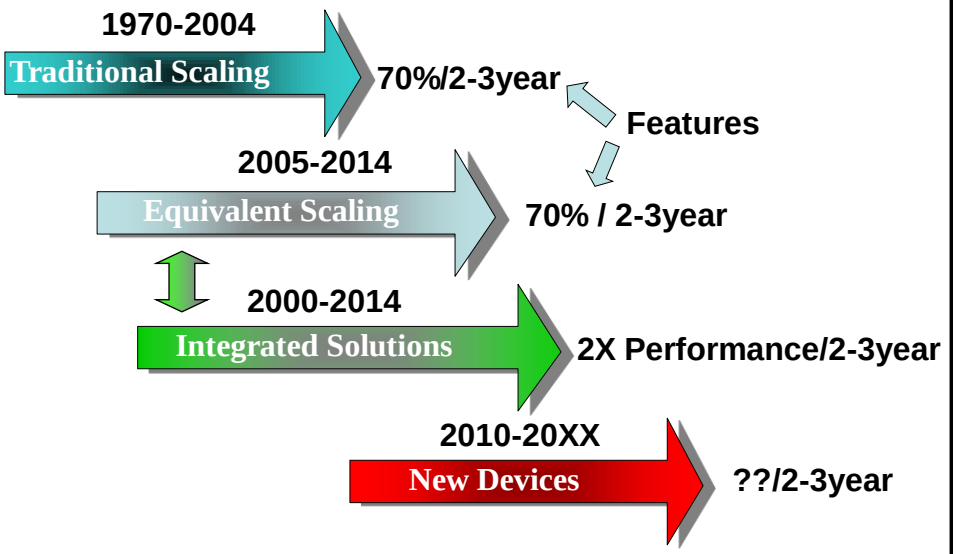
2012/2013 1. félév
Nem-szerkesztett (ideiglenes) változat!

1

DOWN-SCALING INTO THE NANOMETER …

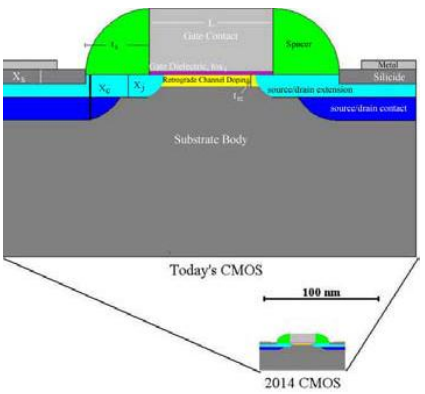


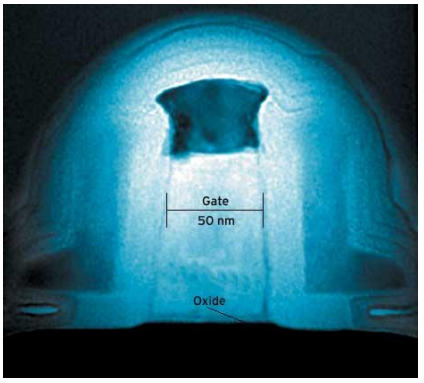
CMOS Future Directions and Beyond



Si NANOELEKTRONIKA

Hol áll az ipar ma, és mi várható a közeljövőben?

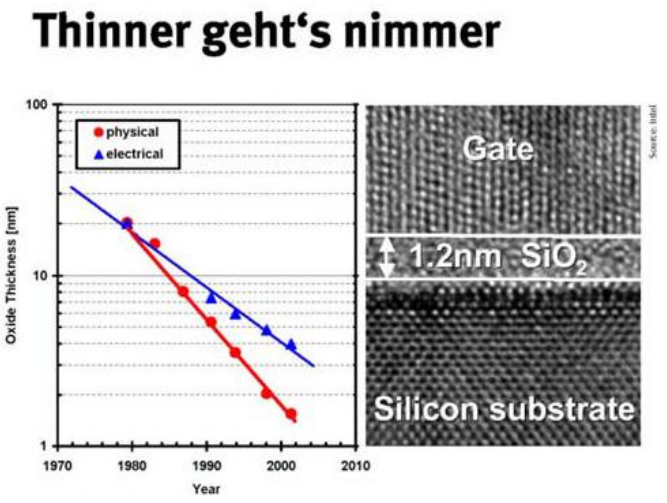




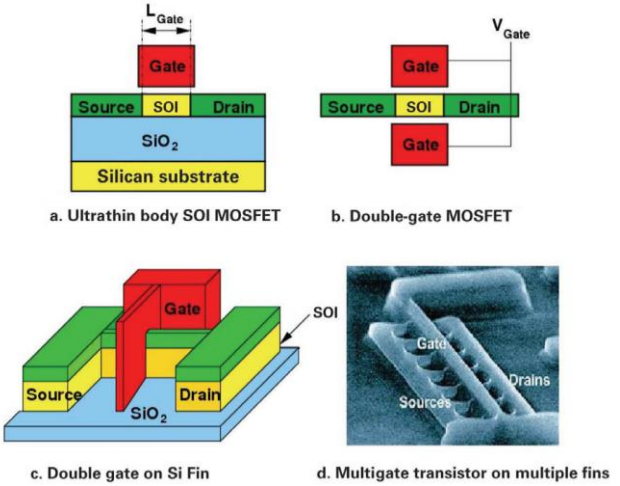
CMOS ma (tegnap?): INTEL

4

A KICSI EGYRE KISEBB LESZ …

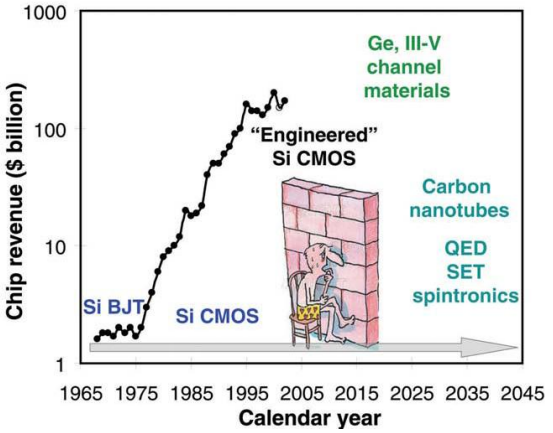


MOSFET A NANOTARTOMÁNYBAN



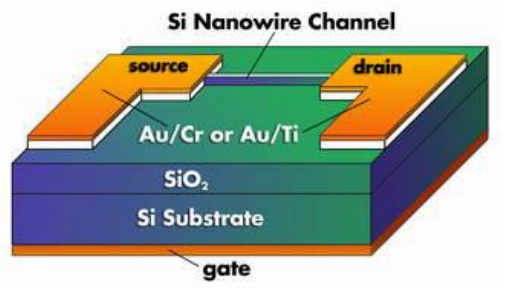
Emerging alternative fully depleted CMOS structures for continued scaling: (a) one-, (b, c) two-, and (d) three-gate fully depleted devices.

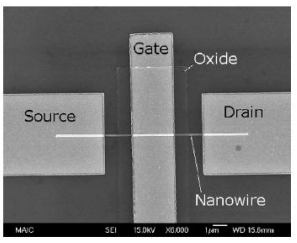
Si TECHNOLÓGIA MEGÚJULÁSA: NANO- ÉS KVANTUMOS ESZKÖZÖK



Si technology industry time line showing semiconductor revenue and the evolution of new devices and possible time frame for new device types (BJT – bipolar junction transistor, QED – quantum electronic device, and SET – single electron transistor).

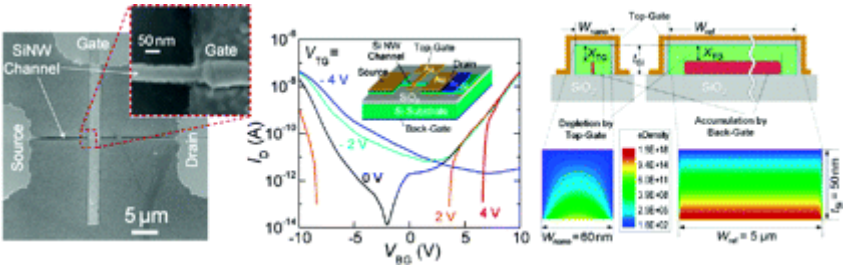
Si NANOHUZAL TRANZISZTOR





Lépték: 1 μm

Si NANOHUZAL TRANZISZTOR



Enhanced Channel Modulation in Dual-Gated Silicon Nanowire Transistors

Si NANOWIRE GATE-ALL-AROUND TRANSISTOR

The foremost issues are:

1. poor gate electrostatic control of the channel potential and thus degraded short-channel effects;

2. high gate leakage due to thin gate dielectric;

3. reduced channel mobility on account of increased doping in the channel; and

4. increased source/drain resistance.

These issues cause higher off-state leakage and limit the drive current leading to compromised performance, defeating the main purpose of scaling.

Si NANOWIRE GATE-ALL-AROUND TRANSISTOR

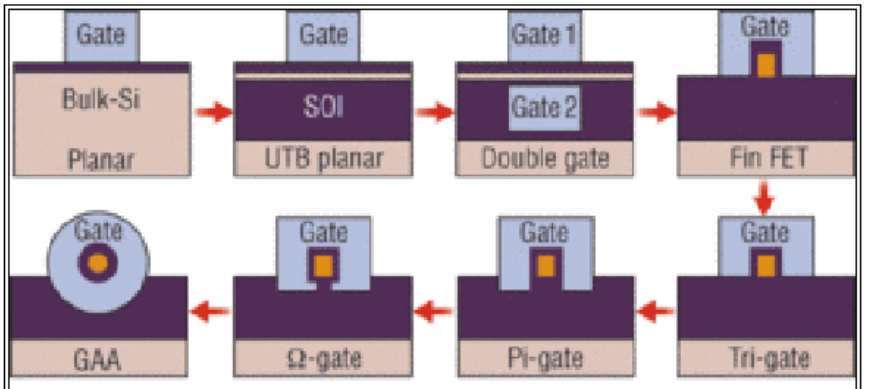


Figure 1. *Progression of device structure from single-gated planar FET to fully gate all around (GAA) MOSFET.*

Si NANOWIRE GATE-ALL-AROUND TRANSISTOR

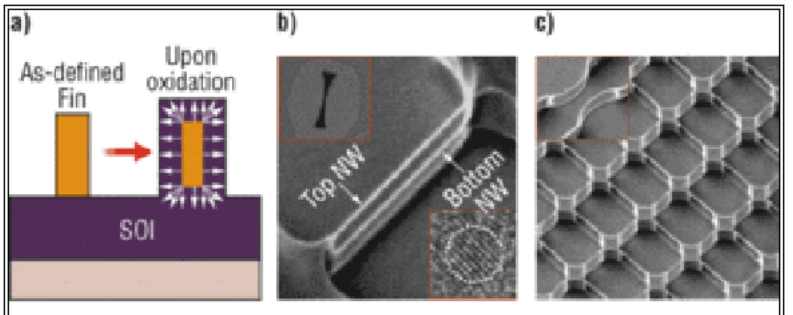
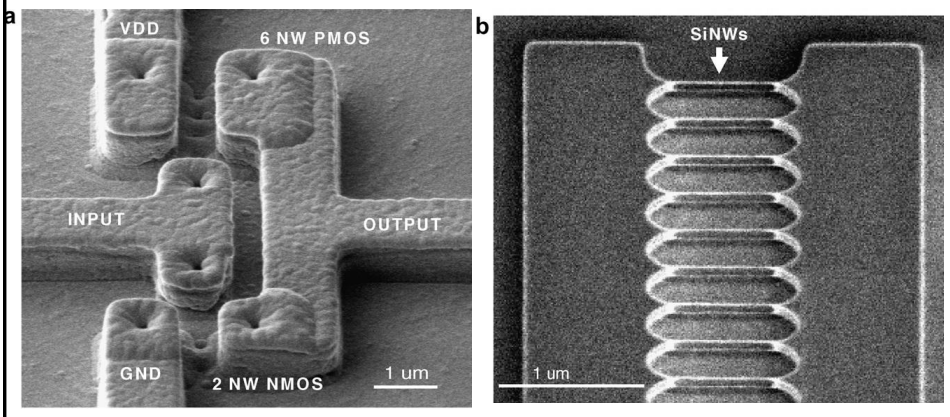


Figure 2. a) *Fin schematics: as-patterned and upon oxidation where arrows are showing the volume expansion direction;* ***b)*** *tilt view image of twin nanowires after removal of grown SiO_2-released nanowires. The insets show a TEM micrograph after stress-limited oxidation just before the fin converts into twin wires (top left) and cross section of nanowire (bottom right);* ***and c)*** *regular network of nanowires and with lithographically defined curved nanowires as inset in the top left corner.*

Si NANOWIRE GATE-ALL-AROUND CMOS INVERTER

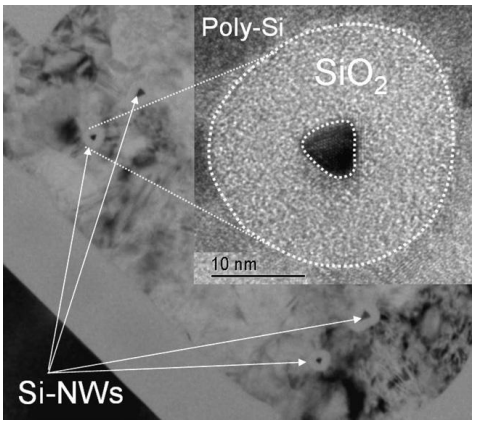
We present the monolithic integration of gate-all-around (GAA) Si-nanowire FETs into CMOS logic using top-down approach. Inverters are chosen as the test vehicles for demonstration. Empirically optimized designs show sharp ON–OFF transitions with high voltage-gains (e.g., $\Delta V_{OUT}/\Delta V_{IN}$ up to ~45) and symmetric pull-up and pull-down characteristics. The matching of the drive currents of n- and p-MOSFETs is achieved using different number of nanowire channels for N- and P-MOS transistors. The inverter maintains its good transfer characteristics and noise margins for wide range of V_{DD} tested down to 0.2 V. The detailed experimental characterization is discussed along with the electrical characteristics of the individual transistors comprising the inverter. The performances of the inverters are discussed vis-à-vis those reported in the literature using advanced non-classical device architectures such as Fin-FETs. The integration potential of GAA Si-nanowire transistors to realize CMOS circuit functionality using top-down approach is thus demonstrated.

Si NANOWIRE CMOS



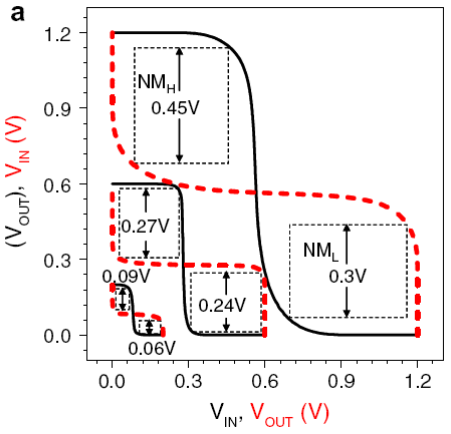
(a) SEM image of the top-down fabricated GAA Si NW inverter showing (1x2) channel N-MOS and (3x2) channel P-MOS. (b) Tilted view of multiple released nanowires in a row showing excellent yield and symmetric wires which are critical for inverter functionality.

Si NANOWIRE CMOS



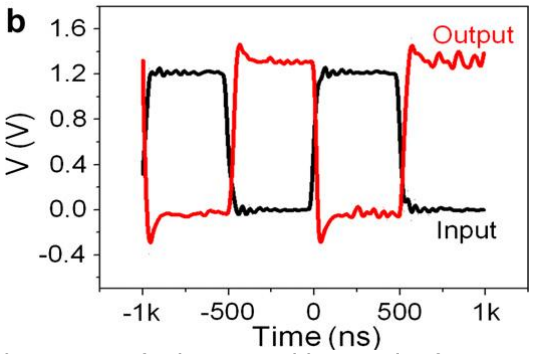
TEM image of GAA P-MOS from the inverter (1:2 N-MOS to P-MOS channel ratio). Inset on top right corner shows the enlarged image of the gate dielectric with 10 nm gate oxide surrounding the silicon NW.

INVERTER TRANSFER CHARACTERISTICS



Transfer characteristics of inverter (1:3 N-MOS to P-MOS channel ratio) at different VDD with VIN and VOUT plotted interchangeably on X- and Y-axis in a butterfly plot.

DYNAMIC RESPONSE



Dynamic (pulse) response for inverter with 50 pair of P-MOS channel and 20 pairs of N-MOS channels at 1 MHz. Output levels clearly reach VDD. The inverter delay turns out to be 64 ps for these long devices. This would scale down to 1 ps for a 20 nm node maintaining all other structural parameters and length ratios and increasing the current by a factor of five for shorter channel which is reasonable.

SZÉN ALAPU (NANO-)ELEKTRONIKA

1.Szén nanocső (CNT) mint az (nano-)elektronika alapanyaga.
(Sokak szerint a szén nanocső (*carbon nanotube, CNT*) lesz a 21. század legfontosabb anyaga. A jövő eldönti, hogy ez igaz lesz-e, da a múlt arra tanít, hogy a legtöbb jóslat nem vált be.)

2. Grafén mint a nanoelektronika alapanyaga
(Sokak szerint ….. ld. az 1. pont …)

SZÉN ALAPU (NANO-)ELEKTRONIKA

Néhány triviális előny:

Nagy töltéshordozó mozgékonyság (gyors működés, magas határfrekvenvcia, stb.)
Kis (nano-)méret (magasfokú integráltság, stb.)
Jó hő(el)vezetés (nagy teljesítényű eszközök)
Stb.,…

Eszközök (amiről írnak, és beszélnek):

Vezetékek
Dióda, tranzisztor (elsősorban FET)
Optoelektronikai eszközök
Elektron emitterek (hidegemisszió)

NÉHÁNY JÖVENDÖLÉS (NEM VÁLTAK BE …)

"I think there is a world market for maybe five computers."

- Thomas Watson
Chairman of IBM, 1943

"Computers in the future may weigh no more than 1.5 tons."

Ez speciel bejött …

- Popular Mechanics, 1949

NÉHÁNY JÖVENDÖLÉS (NEM VÁLTAK BE …)

"There is no reason for any individual to have a computer in their home."

- Ken Olson, President, Chairman and Founder of Digital Equipment Corp., 1977

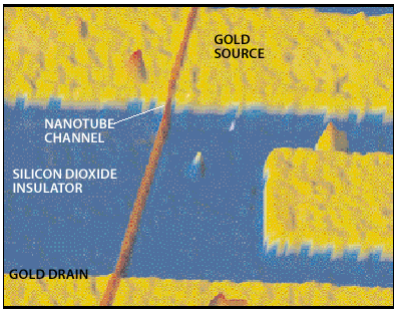
"640K ought to be enough for anybody."

- Bill Gates, 1981 (though today he denies he said it)

SZÉN ALAPÚ (NANO-)ELEKTRONIKA

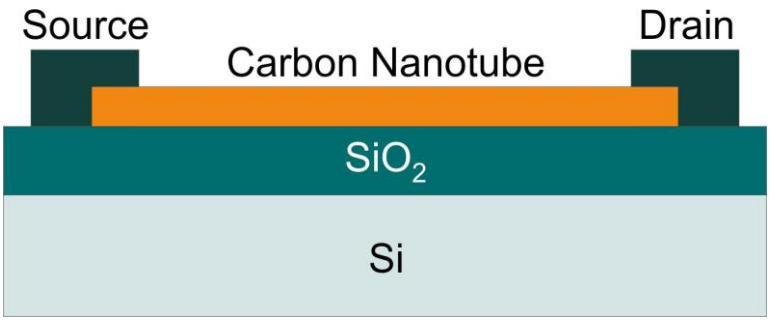
Field-effect transistors based on semiconductor *nanotubes* and *graphene nanoribbons* have already been demonstrated, and metallic nanotubes could be used as high-performance interconnects.

Moreover, owing to the excellent optical properties of nanotubes it could be possible to make both electronic and optoelectronic devices from the same material.



CNT FET: Forrás (source) és nyelő (drain) elektródák: aranycsík, vezetőcsatorna: Szén nanocső (CNT)

SZÉN NANOCSŐ FET



Schematic view of „conventional“ Carbon Nanotube Transistor

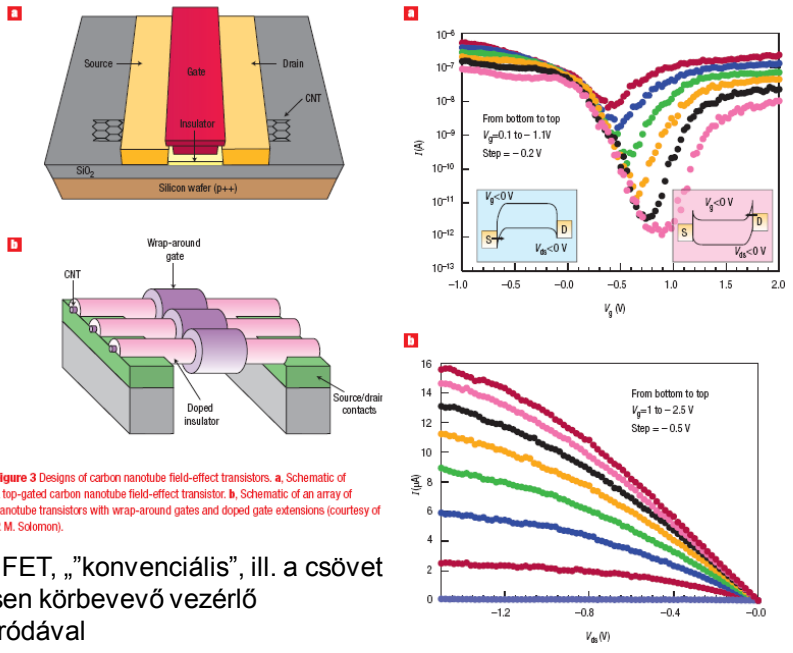
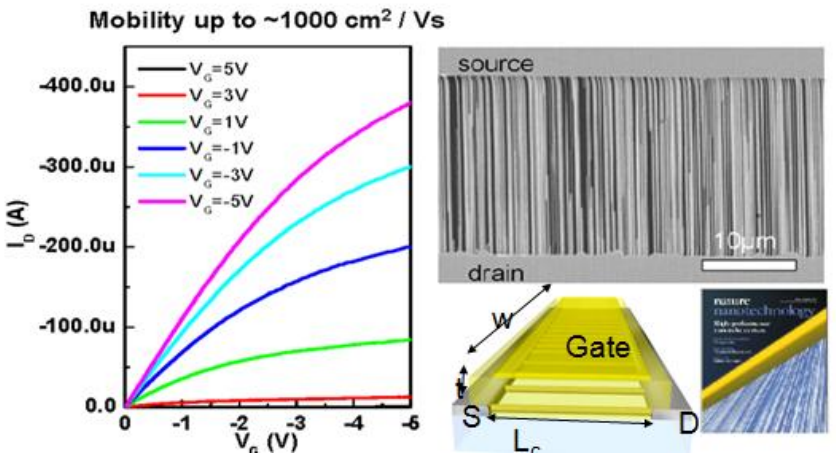


Figure 3 Designs of carbon nanotube field-effect transistors. **a**, Schematic of a top-gated carbon nanotube field-effect transistor. **b**, Schematic of an array of nanotube transistors with wrap-around gates and doped gate extensions (courtesy of P. M. Solomon).

CNT FET, „”konvenciális”, ill. a csövet teljesen körbevevő vezérlő elektródával

SZÉN NANOCSŐ FET TRANZISZTOR

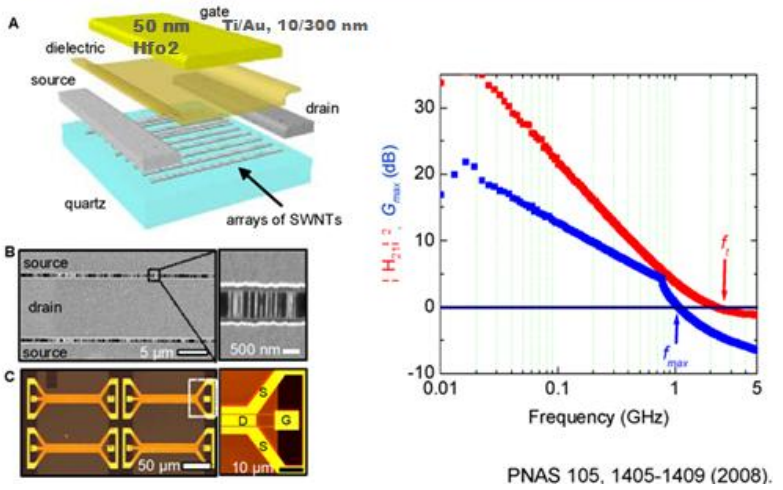
SWNT Array Transistors



A FET tranzisztor vezető csatornáját párhuzamos egyfalú szén nanocsövek (SWNT) alkotják.

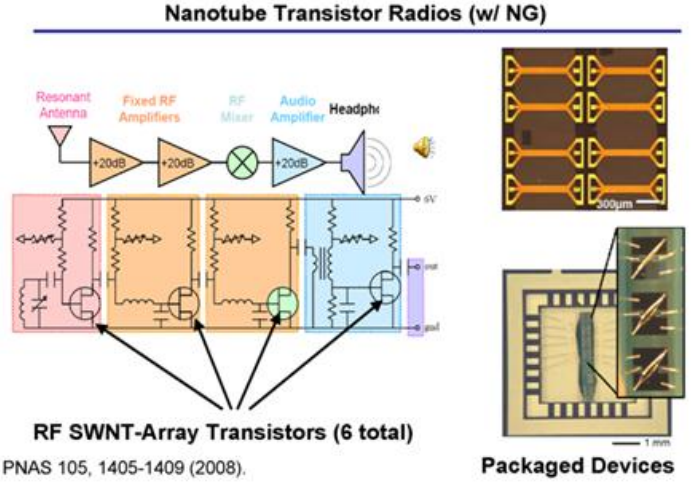
SZÉN NANOCSŐ FET TRANZISZTOR

Nanotube Transistors for RF Analog Electronics (w/ NG)



Párhuzamos szén nanocsövekből álló FET szerkezete és erősítés-frekvencia karakterisztikája.

SZÉN NANOCSŐ-TRANZISZTOROS RÁDIÓ



Felépítés: rezonáns (párhuzamos LC) antenna, két RF erősítő fok (egyenként 20 dB), RF keverő, transzformátor csatolású hangfrekvenciás erősítő (20 dB), fülhallgató

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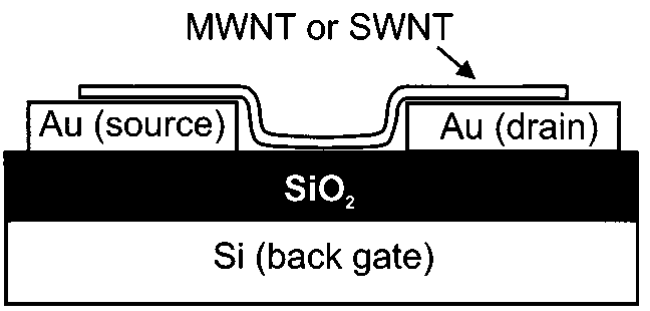
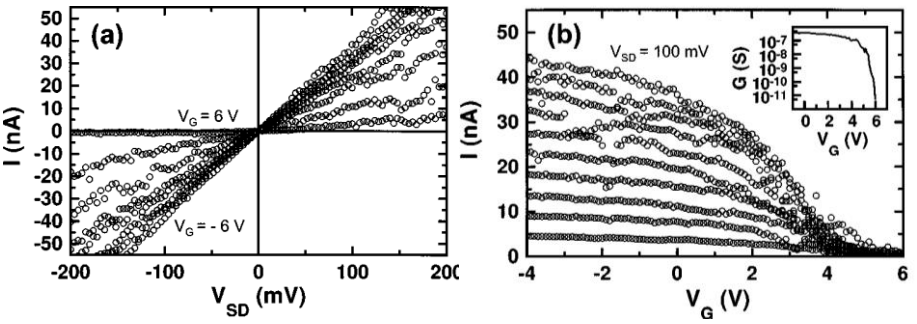
CNT FET



Schematic cross section of the FET devices. A single nanotube (NT) of either multi-wall (MW) or single-wall (SW) type bridges the gap between two gold electrodes. The silicon substrate is used as back gate.

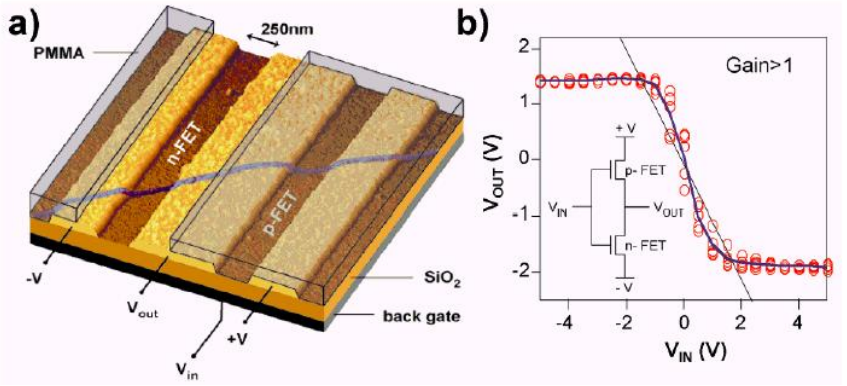
CNT FET CHARACTERISTICS



Output and transfer characteristics of a SWNT-FET: I –V_{SD} curves measured for 0, 1, 2, 3, 4, 5, and 6 V.
I –V_G curves for10– 100 mV in steps of 10 mV.
The inset shows that the gate modulates the conductance by 5 orders of magnitude.

Megfeleltetés: p-csatornás kiürítéses FET

CNT FET INVERTER ÉS LOGIKAI KAPUK

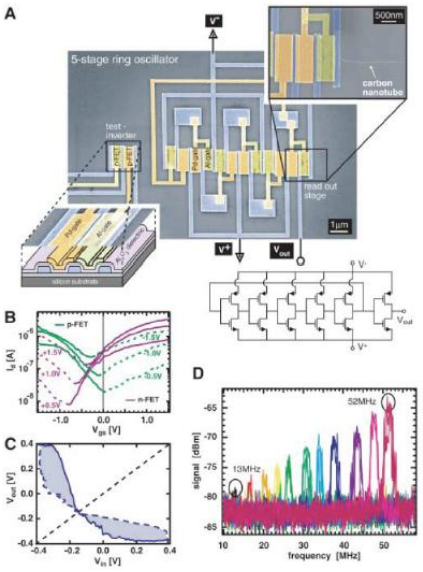


The first CNTFET circuit: inverter circuit
(red circles : results of five measurement series)

CARBON NANOTUBE FET

Transport in the nanotubes is dominated by holes and, at room temperature, it appears to be diffusive. Using the gate electrode, the conductance of a single wall nanotube FET could be modulated by more than 5 orders of magnitude. An analysis of the transfer characteristics of the FETs suggests that the nanotubes have a higher carrier density than graphite and a hole mobility comparable to heavily p-doped silicon.

CNT RING OSCILLATOR



An Integrated Logic Circuit Assembled on a Single Carbon Nanotube

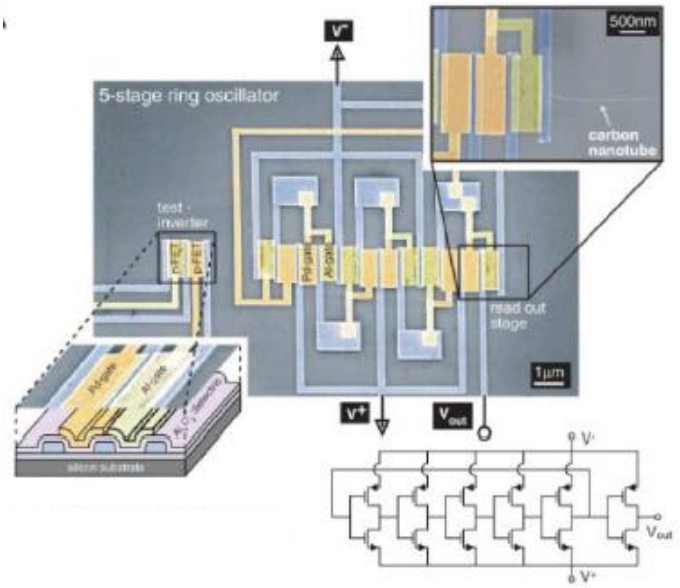
Zhihong Chen,[1] Joerg Appenzeller,[1]* Yu-Ming Lin,[1] Jennifer Sippel-Oakley,[2] Andrew G. Rinzler,[2] Jinyao Tang,[3] Shalom J. Wind,[4] Paul M. Solomon,[1] Phaedon Avouris[1]*

www.sciencemag.org SCIENCE VOL 311 24 MARCH 2006

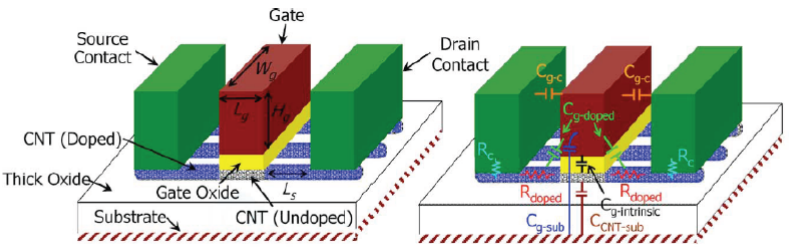
Fig. 1. (**A**) Scanning electron microscope image of a SWCNT ring oscillator consisting of five CMOS inverter stages. A test inverter was added to determine the parameter set for the actual measurement. (**B**) Characteristics for the p-type FET with Pd metal gate and n-type FET with Al gate. (**C**) Inverter characteristics and its mirrored curve. (**D**) Voltage-dependent frequency spectra. From the left to the right, the respective supply voltages are as follows: V_{dd} = 0.5 V and 0.56 V to 0.92 V (in 0.4-V increments).

A gyűrűs oszcillátor páratlan számú (itten öt) inverterből álló lánc visszacsatolással. Az oszcillációs frekvenciát az egyes inverterek terjedési késleltetése határozza meg.

CNT RING OSCILLATOR



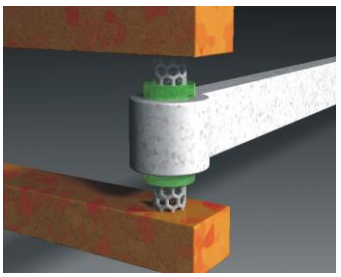
CNT FET



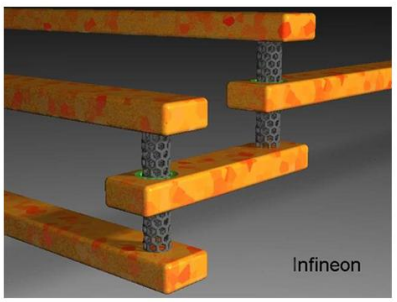
"We have a lot to gain from CNFET-based circuits over 32 nm silicon CMOS as long as we can build circuits and architectures immune to misaligned CNTs and metallic CNTs. It is possible to design robust standard cells with guaranteed correct functionality in the presence of misaligned CNTs. We require an interdisciplinary approach to overcome the problem of metallic CNTs (e.g., to fewer than 8% metallic CNTs). We need to combine novel CNT synthesis/ selection/placement techniques, reliable ways of removing metallic CNTs after CNT growth, together with new circuit and architectural techniques to fully overcome the challenge of metallic CNTs. CNFET technology offers good scalability over silicon CMOS if CNT density can be significantly improved to 250 CNTs/*µm.*" Patil. Mitra, Wong, 2009

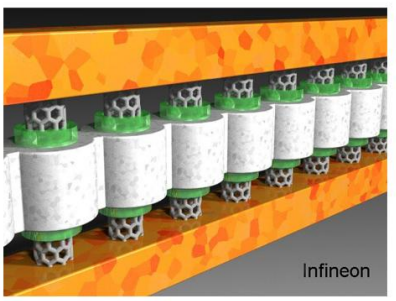
VERTIKÁLIS CNT TRANZISZTOR

Vertical Nanotube Transistor
(Patented by Infineon
- and by Samsung ?!)



Integrated circuits based on semiconductor carbon nanotubes
Compatible with existing „technology”, can extend the period of validity of Moore’s law





Si ÉS CNT ÖSZEHASONLÍTÁS

	CNT FET Seidel (2004)	CNT FET Seidel (2004)	CNT FET Javey (2003)	CNT FET Javey (2004)	CNT FET McEuen (2002)	TriGate Doyle (2003)	FinFET Yu (2002)	SON Harrison (2003)
Channel Material	CNT	CNT	CNT	CNT	CNT	Si	Si	Si
Drive Voltage [V]	0.4	1.0	0.6	0.4	1.0	1.3	1.2	0.9
Drive Current [mA/μm]	15	2.4-6.4	14	11.6	2.96	0.88	0.72	0.914
Transconductance [μS/μm]	4000	2640-6430	3070	17650	6666	920	900	1170
Subthreshold Slope [mV/dec]	200	105	150-170	110	80	69.5	101	70
On Resistance [Ω/μm]	25	155-425	43	22	473	1480	1667	985
Gate Length [nm]	20	600	300	50	1400	60	10	70
Gate Oxide Thickness [nm]	12	8*	67	8	1	1.5	1.7	2
Off Current [nA/μm]	1.0	22**	1.0	600	N/A	120	20	1

GRAFÉN

International Journal of Smart and Nano Materials
Vol. 1, No. 3, August 2010, 201–223

Taylor & Francis
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The evolution of graphene-based electronic devices

Joydeep Basu[a]*, Jayanta Kumar Basu[b] and Tarun Kanti Bhattacharyya[a]

[a]*Department of Electronics and Electrical Communication Engineering;* [b]*Department of Chemical Engineering, Indian Institute of Technology, Kharagpur 721302, India*

(*Received 29 April 2010; final version received 21 July 2010*)

Successful isolation of single-layer graphene, the two-dimensional allotrope of carbon from graphite, has fuelled a lot of interest in exploring the feasibility of using it for fabrication of various electronic devices, particularly because of its exceptional electronic properties. Graphene is poised to save Moore's law by acting as a successor of silicon-based electronics. This article reviews the success story of this allotrope with a focus on the structure, properties and preparation of graphene as well as its various device applications.

Keywords: electronic device; FET; field effect; graphene; nanoelectronics

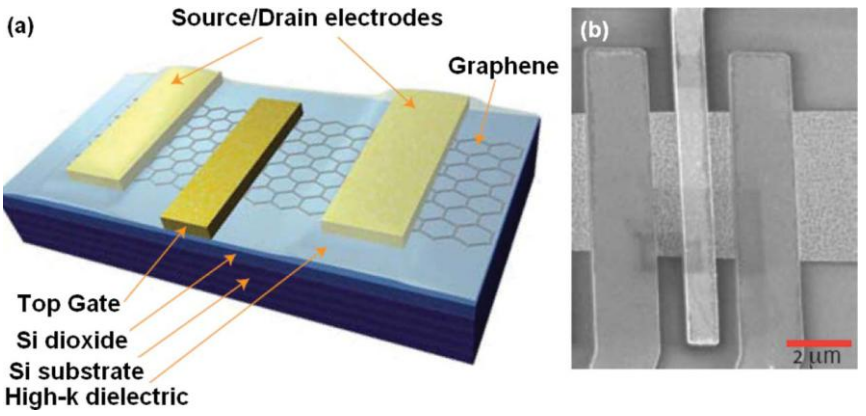
GRAFÉN ELEKTRONIKAI ESZKÖZÖK

Successful isolation of single-layer graphene, the two-dimensional allotrope of carbon from graphite, has fuelled a lot of interest in exploring the feasibility of using it for fabrication of various electronic devices, particularly because of its exceptional electronic properties.

Graphene is poised to save Moore's law by acting as a successor of silicon-based electronics.

Azért itt is érvényes, hogy a jövő eldönti, hogy ez igaz lesz-e, da a múlt arra tanít, hogy a legtöbb jóslat nem vált be…

GRAFÉN FET



A top-gated graphene field effect transistor on a SiO2/Si substrate: (a) schematic diagram;
(b) SEM image

GRAFÉN ÉS FONTOSABB FÉLVEZETŐK TULAJDONSÁGAI

Table 1. Comparison of the properties of graphene with those of some common semiconductors.

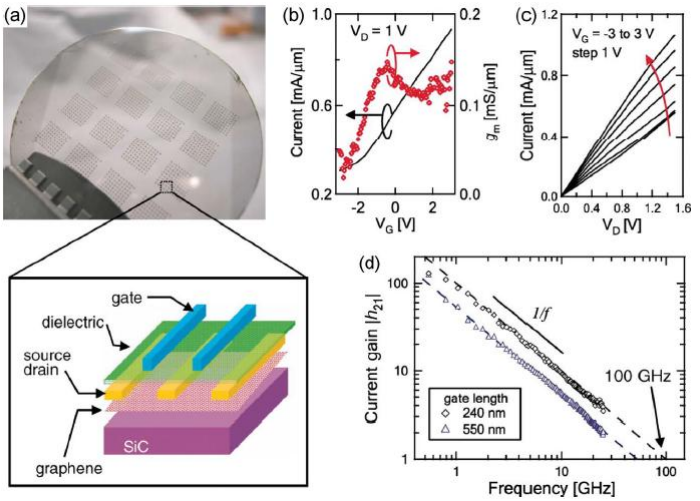
	Graphene	Si	Ge	GaAs	InAs	InP
Electron mobility ($cm^2\ V^{-1}\ s^{-1}$) @ 300 K	200,000	1400	3900	4600	16,000	2800
Band gap energy, E_g (eV)	0	1.12	0.66	1.42	0.36	1.35
Electron saturation velocity V_{sat} (10^7 cm/s)	>5	1	0.6	2.2	4.0	2.2
Density-of-states electron effective mass (m^*/m_o)	0	1.08	0.56	0.067	0.023	0.077
Relative dielectric constant, ε_r	2.4	11.9	16.0	13.1	14.6	12.4
Thermal conductivity ($W\ m^{-1}\ K^{-1}$)	5000	150	60.2	46	27	68
Lattice constant (Å)	2.46	5.43	5.65	5.65	6.06	5.87

BEILLESZTÉS A Si TECHNOLÓGIAI SORBA…

Multilayered epitaxial graphene on insulating SiC substrate has been used for fabricating hundreds of transistors on a single chip. The world's first RF graphene field-effect transistor has been ccomplished using 1–2 layered EG on SiC.

Recently, IBM has reported the creation of top-gated transistors using graphene grown on the silicon face of a 2 inch thick SiC wafer that can operate at speeds of 100 GHz with an electron carrier density of about 3 × 1012 cm−2 and peak mobility of 1500 cm2 V−1 s−1 at room temperature.

This far surpasses the performance of the fastest GaAs transistors.



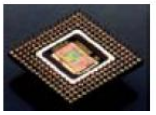
(a) Image and schematic cross-sectional view of the epitaxial graphene FETs. (b) The plot of drain current (ID) and transconductance (gm) of the device with gate voltage (VG) variation at fixed drain bias (VD) of 1 V and the source grounded. (c) The variation of ID as a function of VD for different values of VG. (d) Small-signal current gain (|h21|) variation with frequency.

NANOTECHNOLÓGIA LEHETŐSÉGEI AZ ELEKTRONIKÁBAN

Possible Future Nanotechnologies for Electronics

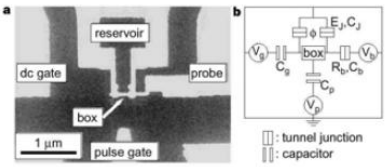
mainstream electronics

top-down
silicon



radically new concepts ...

Quantum Computer



Quantum computation
Solid-state qubits under control ?
D. V. Averin

QUANTUM COMPUTING:
DREAM OR NIGHTMARE?

„The weirdest computer of all" (The Economist)

NANOTECHNOLÓGIA LEHETŐSÉGEI AZ ELEKTRONIKÁBAN

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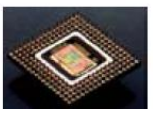

radically new concepts ...

DNA Computer

can solve (some) NP-hard problems
similar to quantum computer
- extremely time consuming

DNA computer in action

NANOTECHNOLÓGIA LEHETŐSÉGEI AZ ELEKTRONIKÁBAN

Possible Future Nanotechnologies for Electronics

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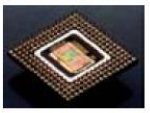
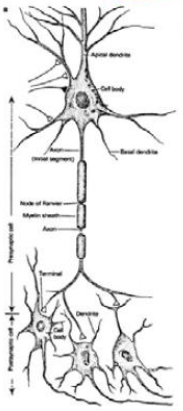
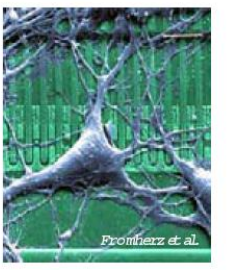
silicon



radically new concepts ...

Brain on Chip





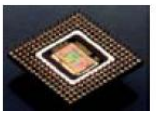
NANO

NANOTECHNOLÓGIA LEHETŐSÉGEI AZ ELEKTRONIKÁBAN

Possible Future Nanotechnologies for Electronics

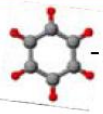
mainstream electronics

top-down
silicon



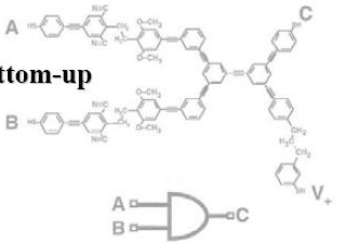
radically new concepts ...

Molecular Electronics



- electronic

bottom-up



KITEKINTÉS

- Nanoelectronics is not only about size but also phenomena, mechanism, etc.
- Nanoelectronics is a wide open field with vast potential for breakthroughs coming from fundamental research.
- Some of the major issues that need to be addressed are:
  - Understand nanoscale transport (theory & experimental).
  - Develop/understand self-assembly techniques to do conventional things cheaper.
  - Find new ways of doing electronics and find ways of implementing them (e.g. quantum computing; hybrid Si-biological systems; cellular automata).