Assessment and subject description

Cubicat mana -	aculty of Ele						onics and Te	redits: 4	
Subject name an Full-time, Fall S	0	ital te	echnics	I.; KMEI	JG	IIAND	C	redits: 4	
Course: Electric		nα							
Responsible:	0	0	7	Teaching	D	. Bálint Pődör, CSc			
Responsible.	esponsible: Dr. Rita Lovassy		/	staff: (honorary) full professo)r		
Prerequisites:				stan.	(II)	onorary) fun professe	Л		
Contact hours	Lecture: 2	,	Class d	iscussion: (<u>)</u>	Lab hours: 0	Tutorial		
per week:	Lecture. 2	-	Class u	1500551011.)	Lao nours. 0	Tutonai	•	
Assessment and	exam								
evaluation:	CXam								
evaluation.			Su	ıbject desc	rin	tion			
Aims. This cours	e will give	an ov				oncepts and applicati	one of digit	al technics	
						acquaint the future e			
	·	-				circuits, and with the	U		
						classroom-tutorials a			
						owledge and suffici			
functioning, oper							ent proneie	ney in th	
v ,	v		<u>.</u>	Ū		Logic (Boolean) algeb	ra logic one	erations	
-			•			is and implementation	U		
						s, code conversion. C			
functional building	÷			•			omomunom	ii on out	
	ig electro, pr	-	Topics	appireation			Week	Lessons	
Fundamental con	cents of digi		-	nd of logic	net	works Specific	VV CCIX		
	indamental concepts of digital technics and of logic networks. Specific aracteristics of digital technics. Digital (binary) representation.						1.	2	
Introduction to a									
connection: textu			0	0		e	2. 2		
algebra: axioms a	-			-	_	-	2.	4	
						gic functions. Fully			
and incompletely specified logic functions. Canonic forms of logic functions. Disjunctive (sum-of-products, SOP), conjunctive (product-of-sum,							3.	2	
POS) canonic for		-		-	neu	(product of sum,			
					łrar	bic representation.			
Manipulation and transformation of logic functions. Graphic representation: Veitch diagrams and Karnaugh maps). The concept and methods of logic						4.	2		
function minimiz				•••••••				_	
		on. O	uine-M	cCluskev a	امما	rithm. Graphic			
i vuinci i cal/tabula		nimization, Quine-McCluskey algorithm. Graphic gh map and applications. Minimization of							
	rnaugh map	and a	pplicati			tion of	_		
minimization, Ka	U 1			ons. Minin	niza		5.	2	
minimization, Ka	cifies logic f	unctio	ons. Syr	ons. Minin	niza		5.	2	
minimization, Ka incompletely spe logic. Simple des	cifies logic f ign/synthesis	unctions exar	ons. Syn nples	ons. Minin nmetric log	niza gic f	functions, XOR		2	
minimization, Ka incompletely spe logic. Simple des Effect of signal p	cifies logic f ign/synthesis ropagation d	unctions exar elays	ons. Syn nples on the o	ons. Minin nmetric log	$\frac{1}{f cc}$	functions, XOR		2	
minimization, Ka incompletely spe logic. Simple des Effect of signal p The concept and	cifies logic f ign/synthesis ropagation d relevance of	unctic s exar lelays hazar	ons. Syn nples on the o ds in lo	ons. Minin nmetric log operation o gic circuits	$\frac{1}{1}$	functions, XOR ombinational logic ne atic hazards (glitches			
minimization, Ka incompletely spe logic. Simple des Effect of signal p The concept and their elimination.	cifies logic f ign/synthesis ropagation d relevance of Functional l	unctions exar elays hazar hazar	ons. Syn nples on the ds in lo ls and th	ons. Minin nmetric log operation o gic circuits heir elimin	$\frac{1}{1}$	functions, XOR ombinational logic ne atic hazards (glitches n.	6.	2	
minimization, Ka incompletely spe logic. Simple des Effect of signal p The concept and their elimination. Number systems,	cifies logic f ign/synthesis ropagation d relevance of Functional l	unctions exar elays hazar hazar	ons. Syn nples on the ds in lo ls and th	ons. Minin nmetric log operation o gic circuits heir elimin	$\frac{1}{1}$	functions, XOR ombinational logic ne atic hazards (glitches	6.		
minimization, Ka incompletely spe logic. Simple des Effect of signal p The concept and their elimination. Number systems, number systems.	cifies logic f ign/synthesis ropagation d relevance of Functional h fundamenta	unctic s exar lelays hazar hazarc ls. Bi	ons. Syr nples on the o ods in lo ls and the nary nu	ons. Minin nmetric log operation o gic circuits heir elimina mbers. Arit	f co f co S. St atio	Functions, XOR ombinational logic ne catic hazards (glitches n. etic operations in the	6.	2	
minimization, Ka incompletely spe logic. Simple des Effect of signal p The concept and their elimination. Number systems, number systems. Codes and encod	cifies logic f ign/synthesis ropagation d relevance of <u>Functional l</u> fundamenta	unctic s exar lelays hazar nazarc ls. Bi	ons. Symples on the ords in loo ls and the nary nu	ons. Minin nmetric log operation o gic circuits heir elimina mbers. Arit	$rac{1}{1}$	Functions, XOR ombinational logic ne satic hazards (glitches n. etic operations in the l alphanumeric	6. 7.	2 2	
minimization, Ka incompletely spe logic. Simple des Effect of signal p The concept and their elimination. Number systems. number systems. Codes and encod codes. Pure binar	cifies logic f ign/synthesis ropagation d relevance of Functional f fundamenta ing, fundame y codes (dire	unctic s exar lelays hazar ls. Bi ental c ect, 1s	ons. Symples on the ords in lo ds and the nary nu concepts complete	ons. Minin nmetric log operation o gic circuits heir elimina mbers. Arit s. Numeric ement, 2s c	riza gic f f co atio thm and omp	Functions, XOR ombinational logic ne satic hazards (glitches n. etic operations in the l alphanumeric	6.	2	

Digital logic functional building blocks I. Encoders and decoders. Simple code changing combinational circuits. Binary/BCD and BCD/binary decoders. Gray code, binary/Gray, Gray/binary decoders. Encoding: error detection and correction, parity bit.	9.	2
Digital logic functional building blocks II. Multiplexers, demultiplexers, comparithmetic elements, half-adder, full adder.	10.	2
Combinational logic design examples. 1-bit model arithmetic logic unit (ALU), 4-bit comparator, priority decoder, etc. Logic design using multiplexers.	11.	2
Realization of combinational circuits using memory elements. Programmable logic devices, PLDs	12.	2
End-of-term review.	13.	2

Assessment and evaluation

The attendance of the lectures is compulsory. Students whose absence from lectures exceeds the limits stipulated in the Rules and Regulations of the University cannot be admitted to examination. The coursework comprises several home assignments and a written mid-term test. Home assignments should be prepared according to the deadlines set. The condition for admission to examination, besides the above rules concerning lecture attendance, is the submission of all home assignments and at least a *pass* mark (2) in the test.

The results of home assignments and of the test will be appropriately incorporated in the final grade. Weighing (app.): home assignments results 20 %, mid-term test result 20%, and exam paper 60 %.

Supplement: According to the Rules and Regulations of the University

Written and oral examination at the end of the semester.

The threshold for pass mark (including the results of home assignments and mid-semester test) is 55 %.

Suggested material

Arató Péter: Logikai rendszerek tervezése, Tankönyvkiadó, Budapest, 1990, Műegyetemi Kiadó 2004

Zsom Gyula: Digitális technika I, Műszaki Könyvkiadó, Budapest, 2000, (KVK 49-273/I). (Can be found on and downloaded from the internet.)

Rőmer Mária: Digitális rendszerek áramkörei, Műszaki Könyvkiadó, Budapest, 1989, (KVK 49-223).

Rőmer Mária: Digitális technika példatár, KKMF 1105, Budapest 1999.

Gál Tibor: Digitális rendszerek I, II, Műegyetemi Kiadó, Budapest, 2002, 2003.

Bálint Pődör: Digital technics I (course materials for 1st year English language course), mti.kvk.uniobuda.hu

Bálint Pődör: Digital technics (course materials for final year elective English language course), mti.kvk.uni-obuda.hu